

ABIT - M514 SCHEMATICS

Version: 0.2

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Model	Features
AW8D-MAX	AC2005, Silent OTES 2, IEEE1394, Dual SATAII 3G RAID, Dual PCIE GbE
AW8D	AC2005, Silent OTES 2, IEEE1394, SATAII 3G RAID, PCIE GbE

```

graph LR
    A["VCCP  
PWM  
ISL6556BCRZ"] <-->|4 PHASE  
SWITCHING  
POWER| B["VRD 10.1  
CPU VCCP"]
  
```



```

graph LR
    VRD10.1[VRD 10.1] <--> P4LGA775[P4 LGA775]
    P4LGA775 <--> CK410[CK410]
    P4LGA775 --- 1A[1A]
    P4LGA775 --- 1B[1B]
    P4LGA775 --- 1C[1C]
  
```



ICH7 GPIO SETTING

Pin Name	Power Well	Usage	Default
GPIO0	Vcc3_3	SM_BUSY(NC)	GPI
GPIO1	5VREF	PREQ#5	GPI
GPIO2	5VREF	PIRQ#E	GPI
GPIO3	5VREF	PIRQ#F	GPI
GPIO4	5VREF	PIRQ#G	GPI
GPIO5	5VREF	PIRQ#H	GPI
GPIO6	Vcc3_3	ACZ_DET	GPI
GPIO7	Vcc3_3	66_DET	GPI
GPIO8	VccSus3_3	LPC_PME#	GPI
GPIO9	VccSus3_3	LAN1_WAKE#	GPI
GPIO10	VccSus3_3	FWH_WP#	GPI
GPIO11	VccSus3_3	SMB_ALERT	Native
GPIO12	VccSus3_3	1394_PME#	GPI
GPIO13	VccSus3_3	LAN2_WAKE#	GPI
GPIO14	VccSus3_3	No connect	GPI
GPIO15	VccSus3_3	No connect	GPI
GPIO16	Vcc3_3	No connect	GPO
GPIO17	Vcc3_3	PGNT#5	GPO
GPIO18	Vcc3_3	No connect	GPO
GPIO19	Vcc3_3	SATA1GP	GPI
GPIO20	Vcc3_3	No connect	GPO
GPIO21	Vcc3_3	SATA0GP	GPI
GPIO22	Vcc3_3	PREQ#4	Native
GPIO23	Vcc3_3	LDRQ1#(NC)	Native
GPIO24	VccSus3_3	No connect	GPO
GPIO25	VccSus3_3	No connect	GPO
GPIO26	VccSus3_3	Energy Lake Tech.(RSVD)	GPO
GPIO27	VccSus3_3	Energy Lake Tech.(STATE0)	GPO
GPIO28	VccSus3_3	Energy Lake Tech.(STATE1)	GPO
GPIO29	VccSus3_3	OC5#	Native
GPIO30	VccSus3_3	OC6#	Native
GPIO31	VccSus3_3	OC7#	Native
GPIO32	Vcc3_3	No connect	GPO
GPIO33	Vcc3_3	Model_DET	GPO
GPIO34	Vcc3_3	Model_DET	GPO
GPIO35	Vcc3_3	No connect	GPO
GPIO36	Vcc3_3	SATA2GP	GPI
GPIO37	Vcc3_3	SATA3GP	GPI
GPIO38	Vcc3_3	MODE_DET	GPI
GPIO39	Vcc3_3	No connect	GPI
GPIO40~47	N/A	Not Implemented	N/A
GPIO48	Vcc3_3	PGNT#4	Native
GPIO49	V_CPU_IO	H_PWRGD	Native

PCI DEVICE SETTING

DEVICE	PCI1	1394
INTA	F	B
INTB	G	
INTC	H	
INTD	E	
IDSEL	21	18
REQ/GNT	1	0

W83303AG Voltage Adjust Table

a.CR01 (VPCI Voltage Setting Register, Default 0x00h, Read/Write)

Bit2	Bit1	Bit0	V1P5_MCH
0	0	0	1.50V
0	0	1	1.55V
0	1	0	1.60V
0	1	1	1.65V
1	0	0	1.70V
1	0	1	1.80V
1	1	0	1.90V
1	1	1	2.00V

b.CR02(VRAM Voltage Setting Register,Default x000 0000b,Read/Write)

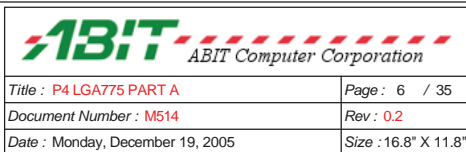
Bit 7 is reserved for signal DDRDET# setting (Dynamic Detect)

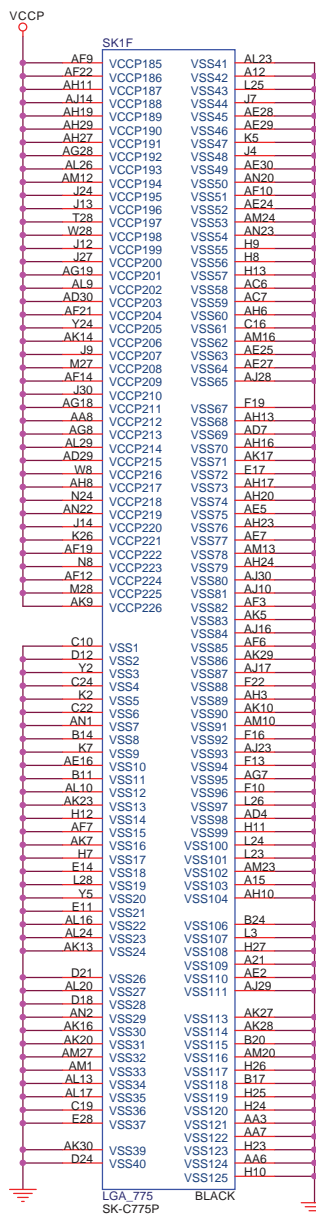
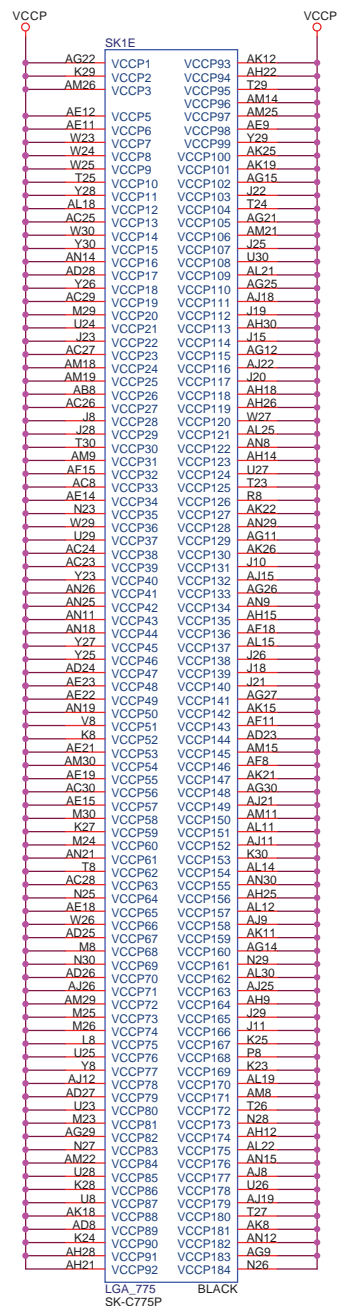
DDRDET# = HIGH bit7 = 1 DDR II type

Low bit7 = 0 DDR type

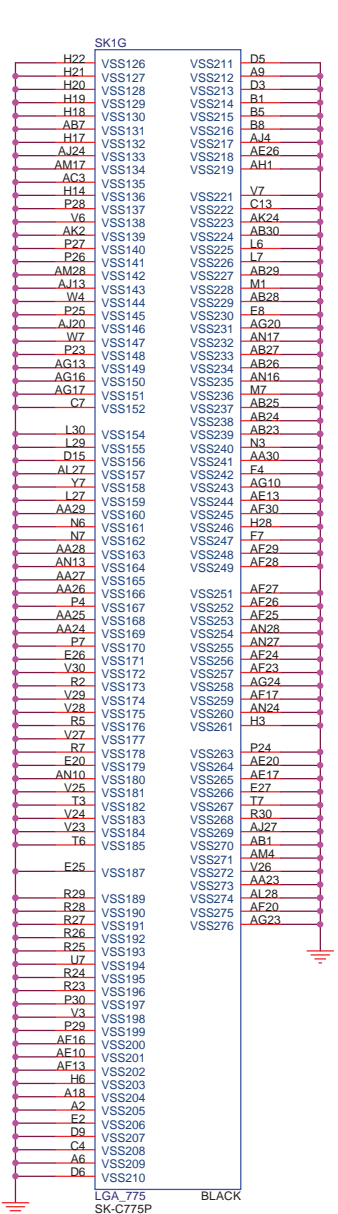
Bit7	Bit3	Bit2	Bit1	Bit0	VDDMEM
1	0	0	0	0	1.80V
1	0	0	0	1	1.75V
1	0	0	1	0	1.85V
1	0	0	1	1	1.90V
1	0	1	0	0	1.95V
1	0	1	0	1	2.00V
1	0	1	1	0	2.05V
1	0	1	1	1	2.10V
1	1	0	0	0	2.20V
1	1	0	0	1	2.30V

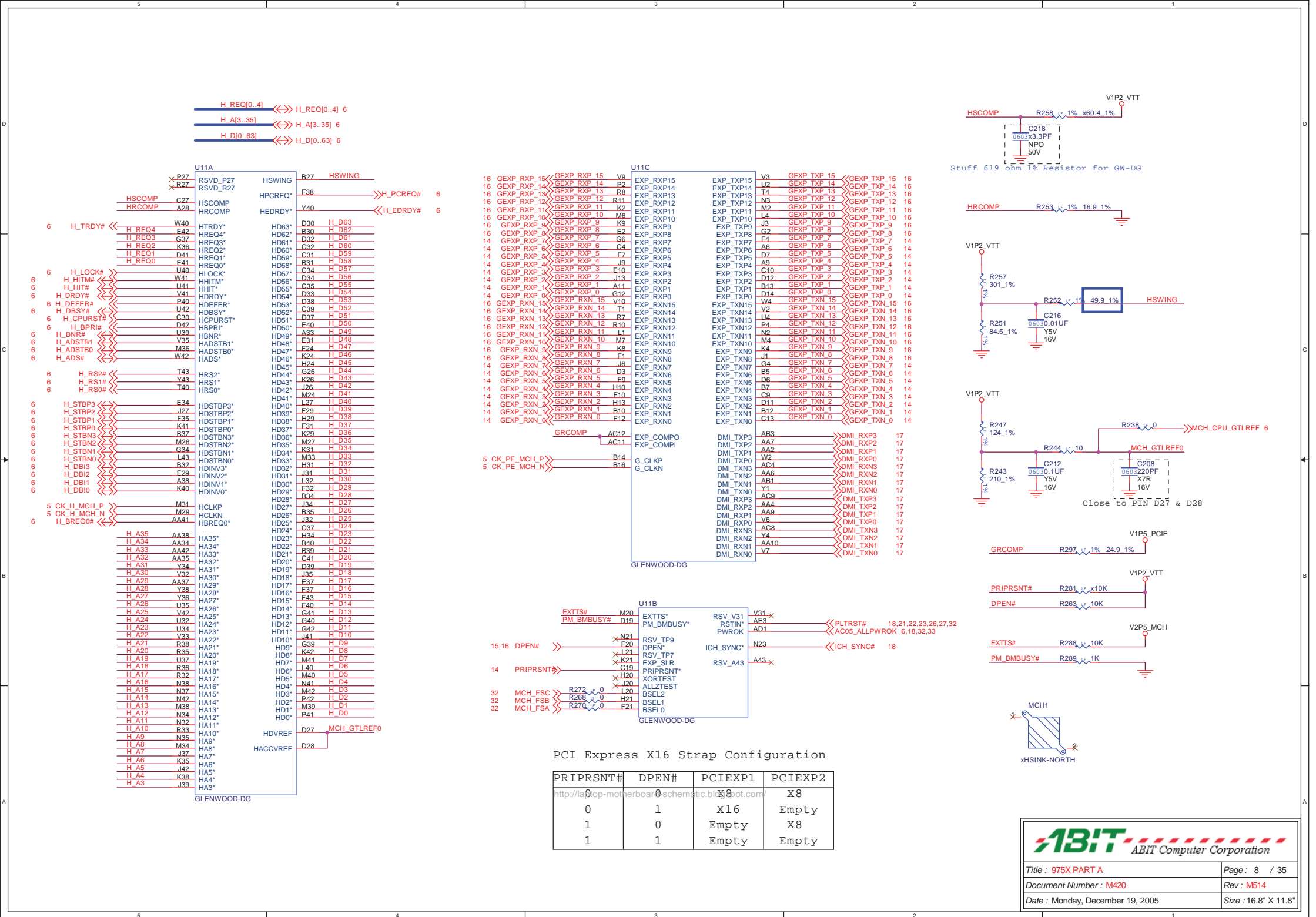
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<http://laptop-motherboard-schematic.blogspot.com/>



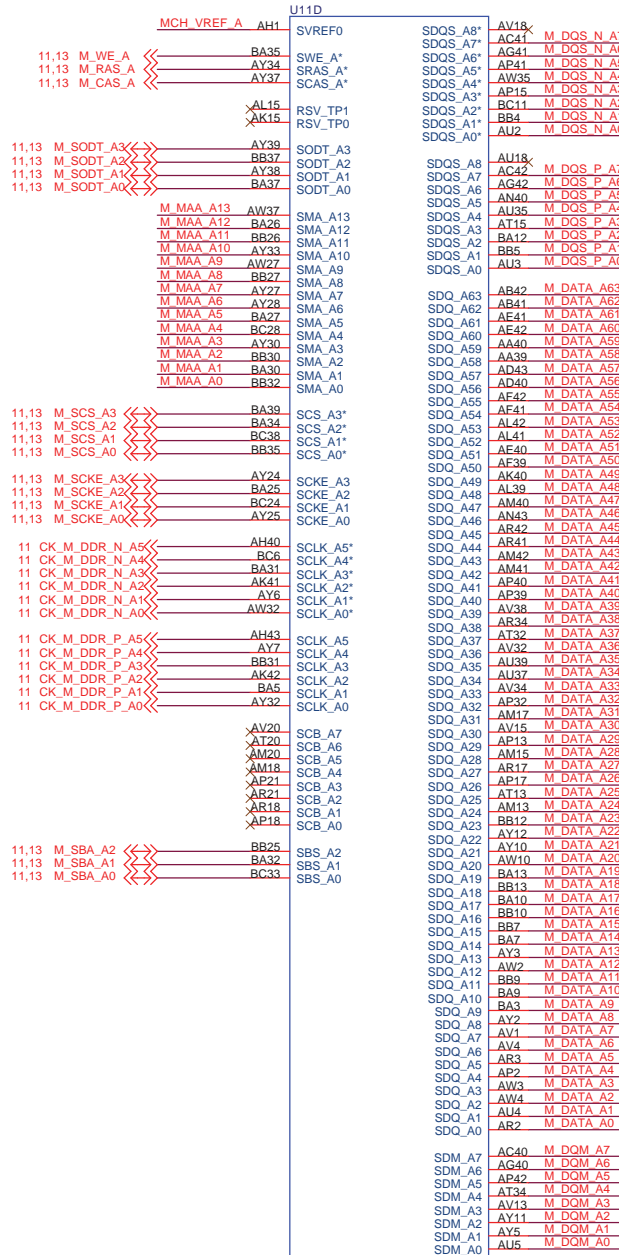


M_MAA_A[0..13] <=> M_MAA_A[0..13] 11,13
M_DQS_P_A[0..7] <=> M_DQS_P_A[0..7] 11
M_DQS_N_A[0..7] <=> M_DQS_N_A[0..7] 11
M_DATA_A[0..63] <=> M_DATA_A[0..63] 11

M_MAA_B[0..13] <=> M_MAA_B[0..13] 12,13
M_DQS_P_B[0..7] <=> M_DQS_P_B[0..7] 12
M_DQS_N_B[0..7] <=> M_DQS_N_B[0..7] 12
M_DATA_B[0..63] <=> M_DATA_B[0..63] 12

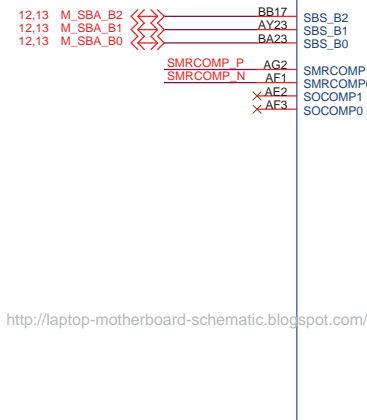
M_MAA_B[0..13] <=> M_MAA_B[0..13] 12,13
M_DQS_P_B[0..7] <=> M_DQS_P_B[0..7] 12
M_DQS_N_B[0..7] <=> M_DQS_N_B[0..7] 12
M_DATA_B[0..63] <=> M_DATA_B[0..63] 12

M_DQS_P_B[0..7] <=> M_DQS_P_B[0..7] 12
M_DQS_N_B[0..7] <=> M_DQS_N_B[0..7] 12
M_DATA_B[0..63] <=> M_DATA_B[0..63] 12

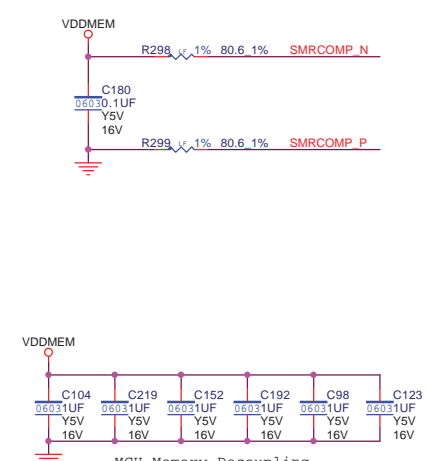
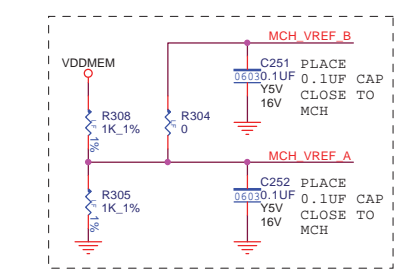
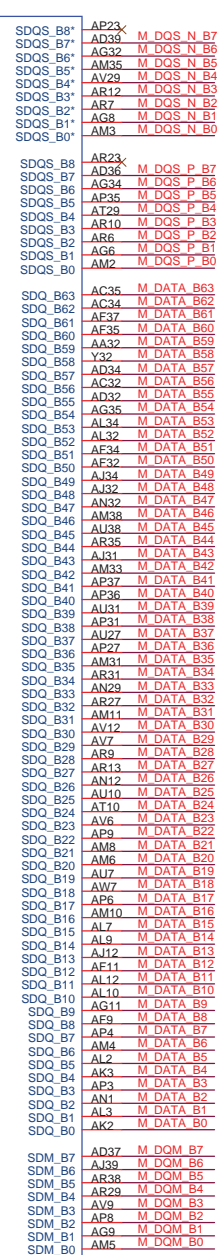


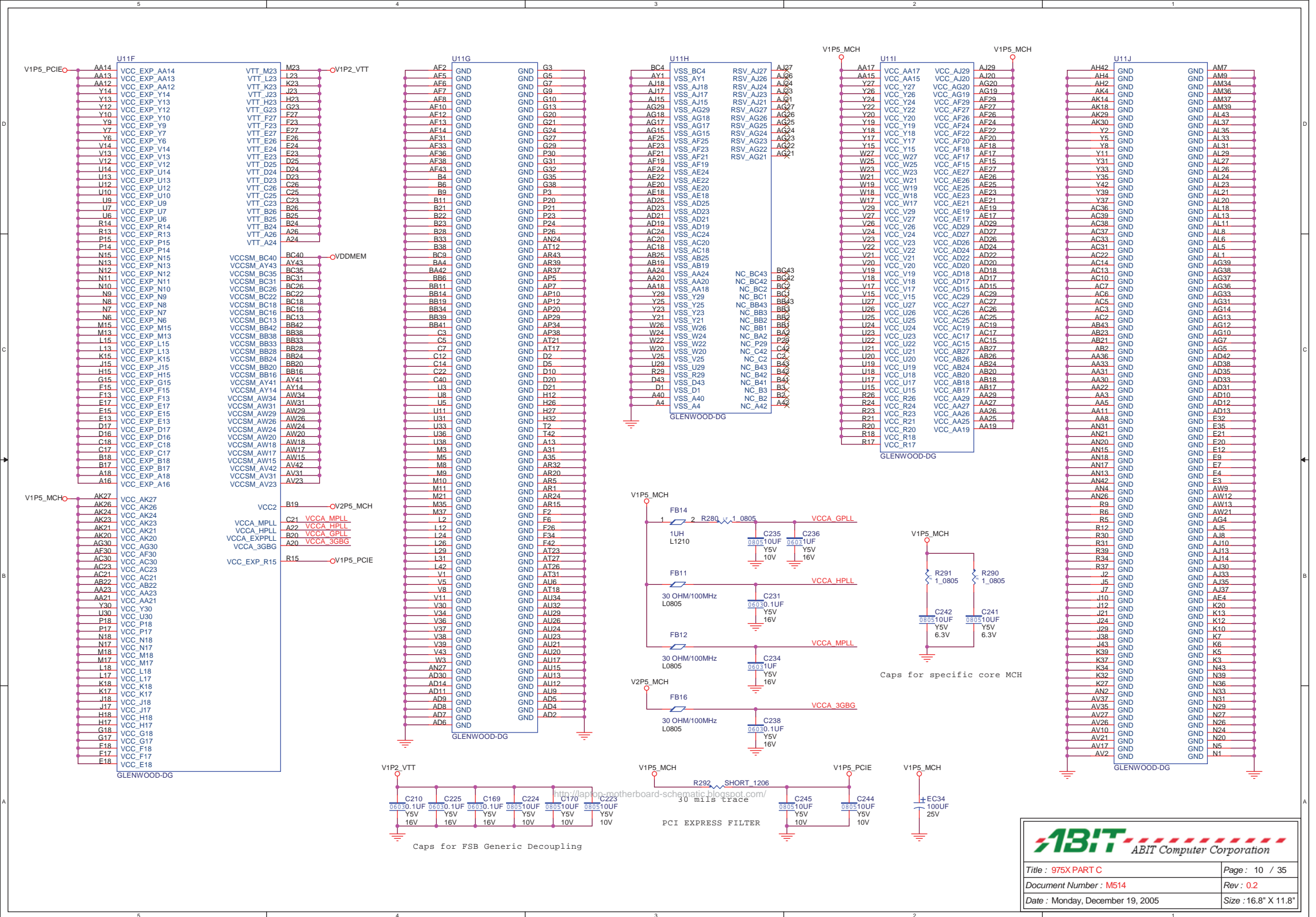
GLENWOOD-DG

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GLENWOOD-DG



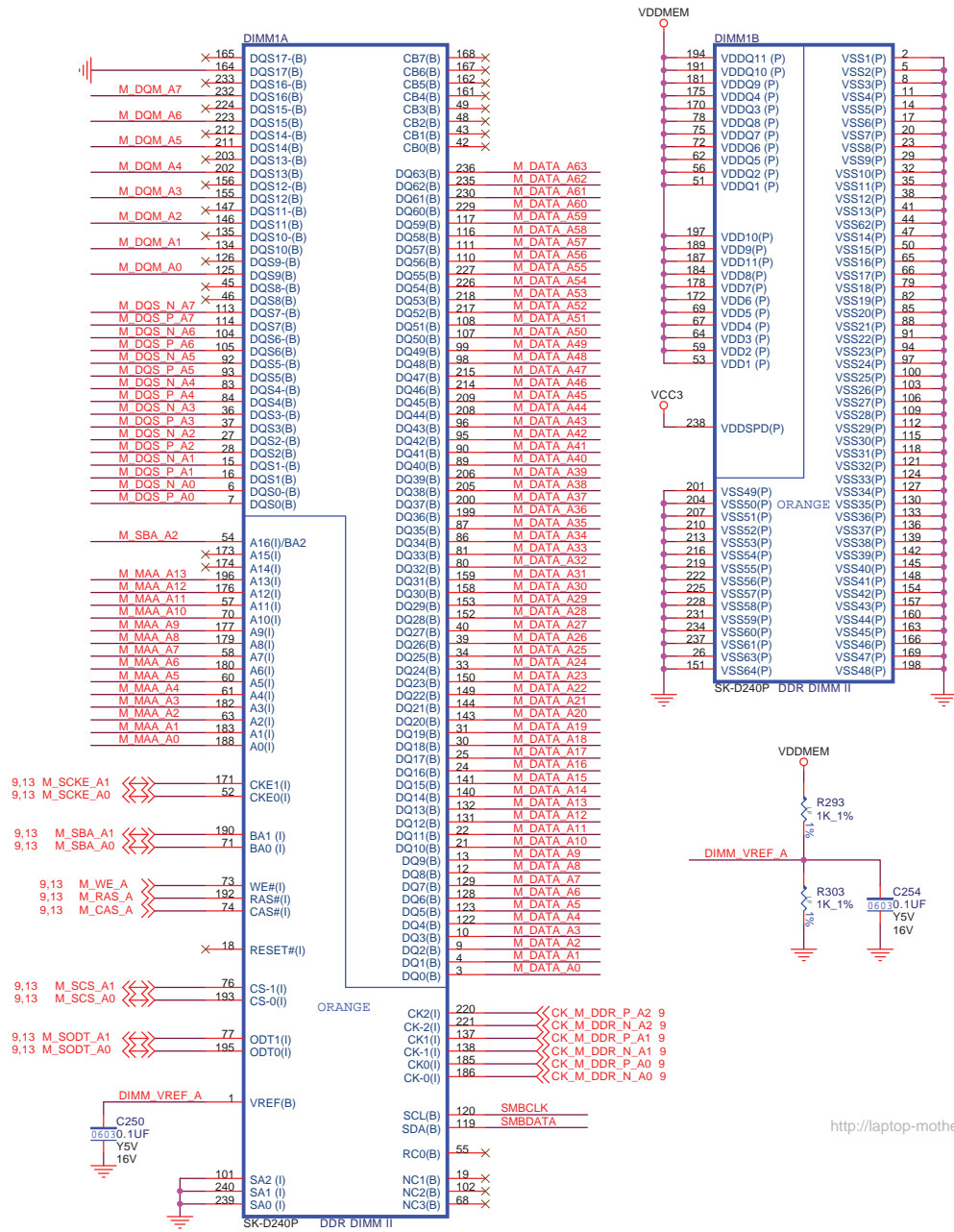


M_DOM A[0..7] <=> M_DOM_A[0..7] 9
M_DATA A[0..63] <=> M_DATA_A[0..63] 9

M_MAA A[0..13] <=> M_MAA_A[0..13] 9,13
M_DQS_P A[0..7] <=> M_DQS_P_A[0..7] 9
M_DQS_N A[0..7] <=> M_DQS_N_A[0..7] 9

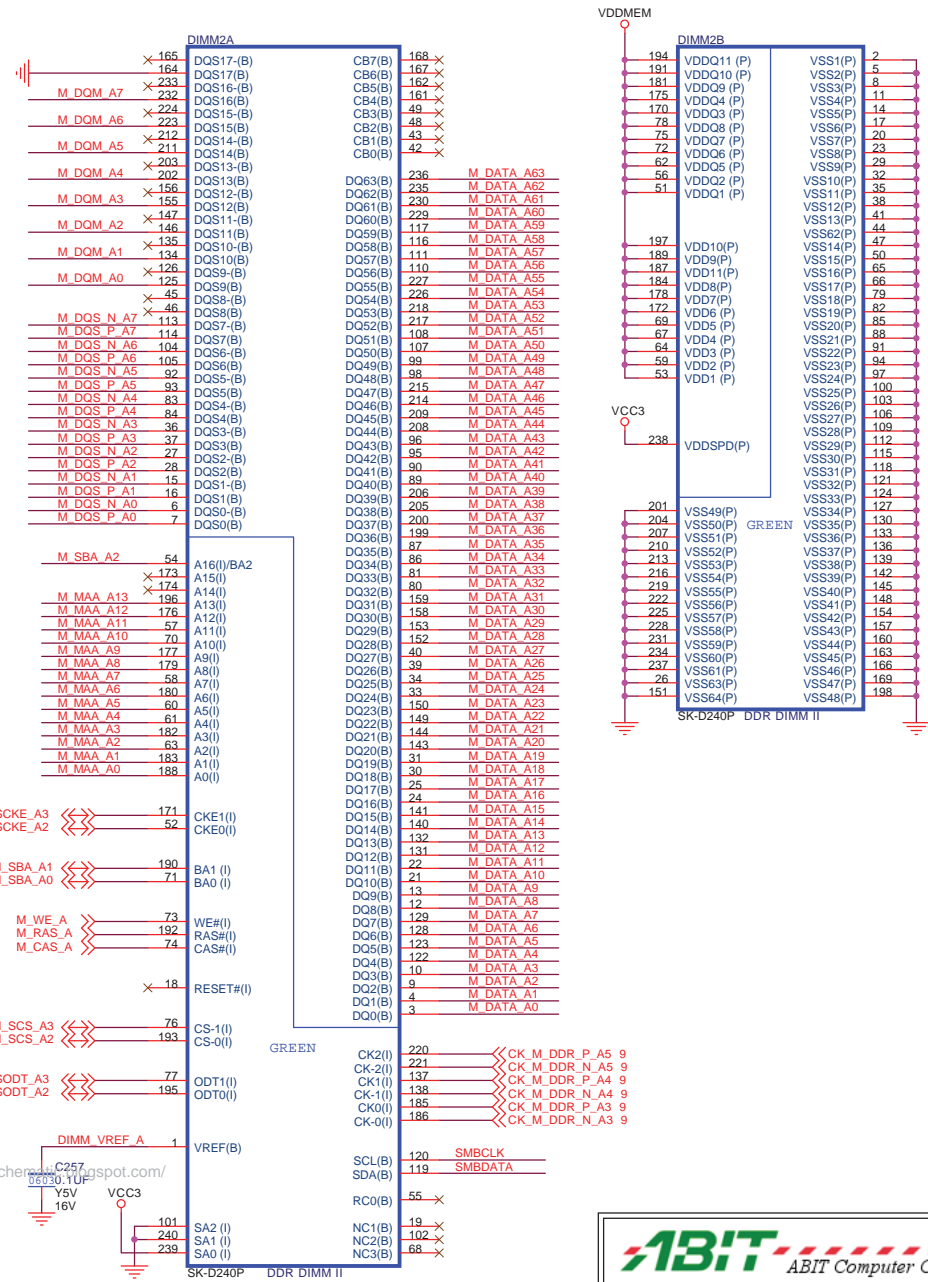
M_SBA_A2 <=> M_SBA_A2 9,13
SMBDATA <=> SMBDATA 12,14,15,18,20,25,26
SMBCLK <=> SMBCLK 12,14,15,18,20,25,26

Channel A DIMM1



ADDRESS=000

Channel A DIMM2



ADDRESS=001

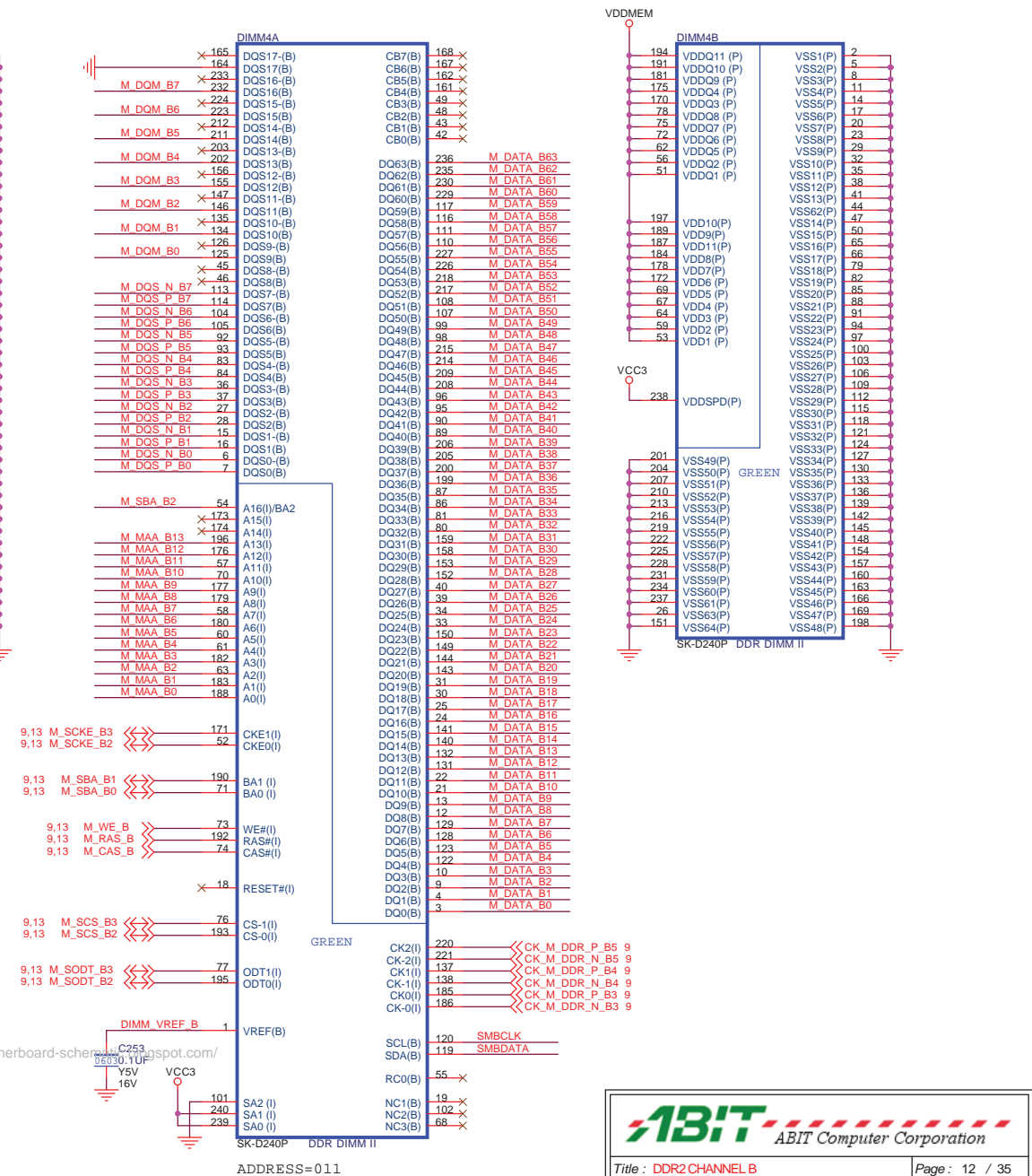
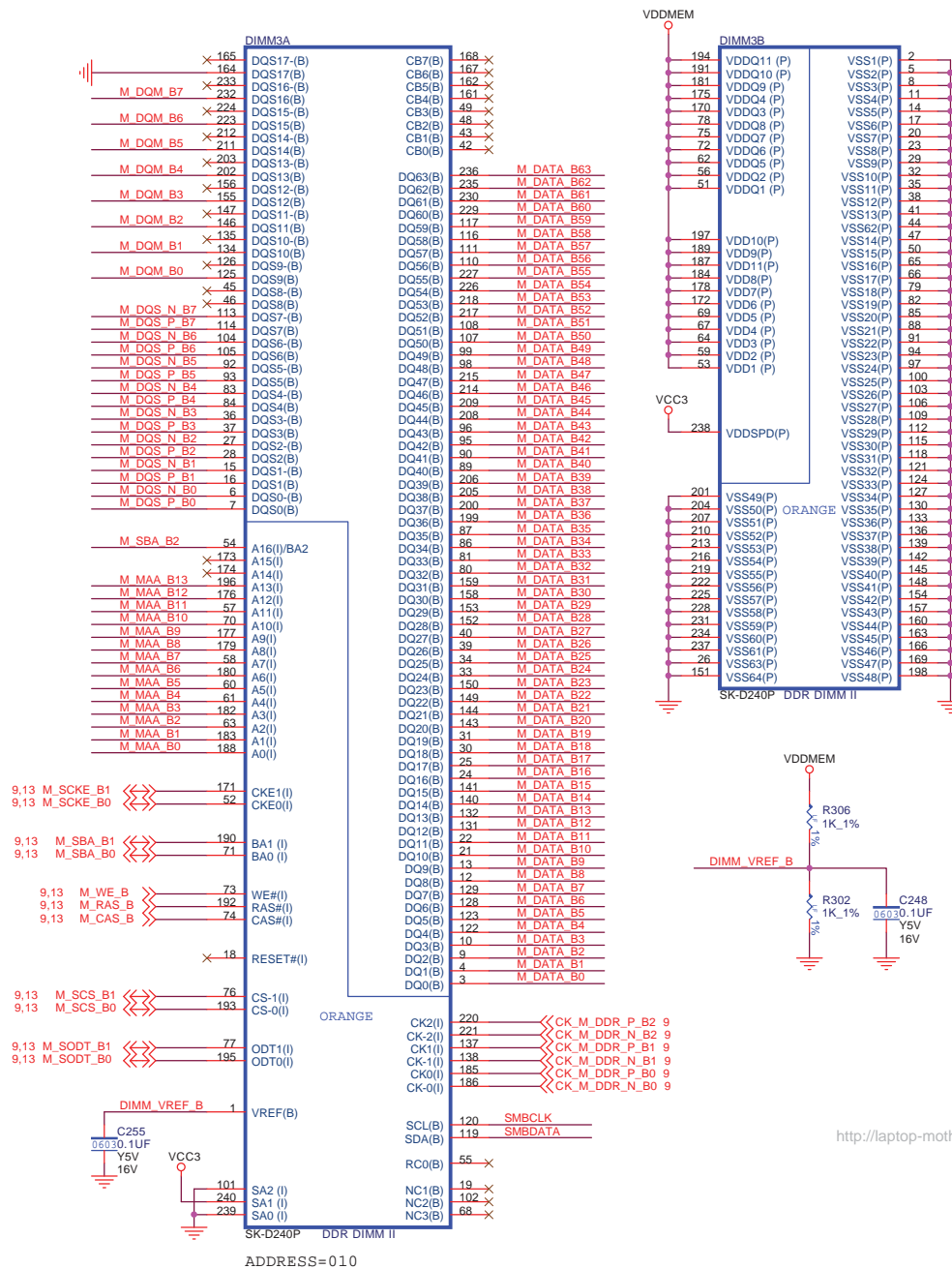
M_DQM_B[0..7] <==> M_DQM_B[0..7] 9
M_DATA_B[0..63] <==> M_DATA_B[0..63] 9

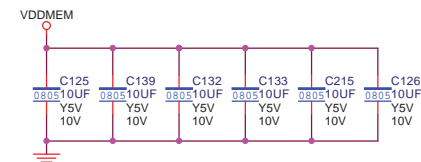
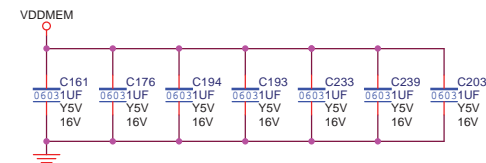
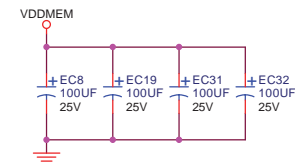
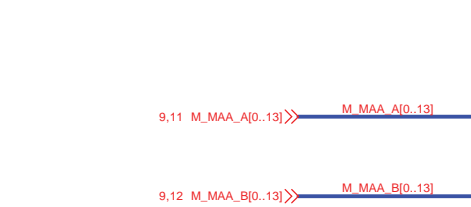
M_MAA_B[0..13] <==> M_MAA_B[0..13] 9,13
M_DQS_P_B[0..7] <==> M_DQS_P_B[0..7] 9
M_DQS_N_B[0..7] <==> M_DQS_N_B[0..7] 9

M_SBA_B2 <==> M_SBA_B2 9,13
SMBDATA <==> SMBDATA 11,14,15,18,20,25,26
SMBCLK <==> SMBCLK 11,14,15,18,20,25,26

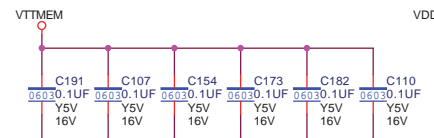
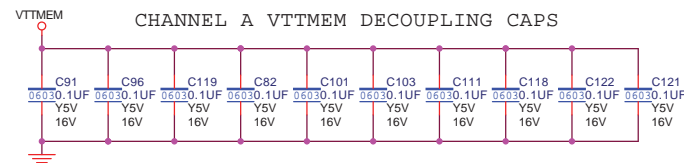
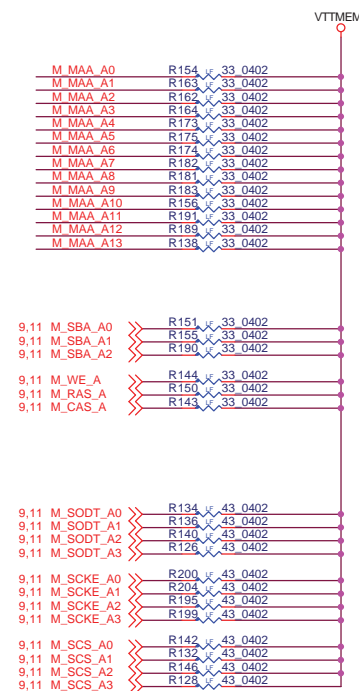
Channel B DIMM1

Channel B DIMM2

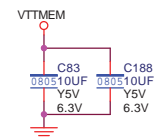




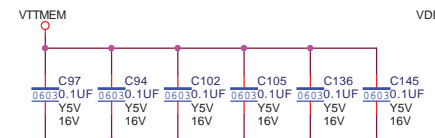
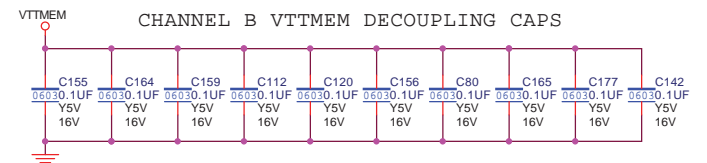
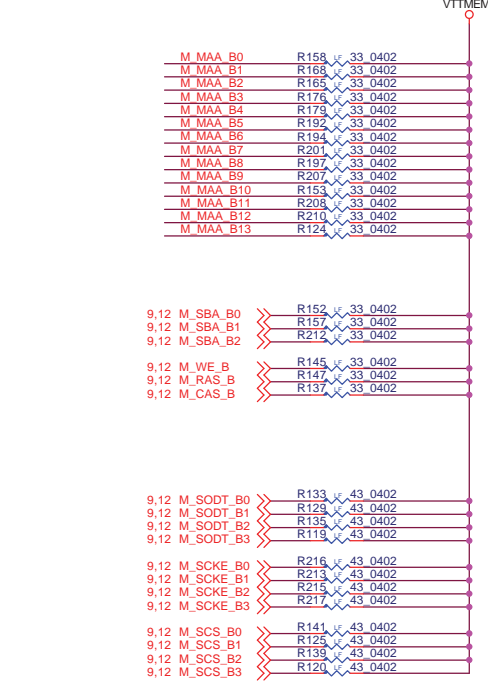
Place Near DIMM



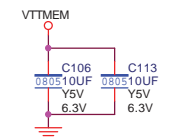
Channel A Address/Control stitching Caps



place at left and right ends of VTT island



Channel B Address/Control stitching Caps



place at left and right ends of VTT island

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8	GEXP_TXP_0	C375	0.1UF	GEXP_TXP_C_0
8	GEXP_TXN_0	C376	0.1UF	GEXP_TXN_C_0
8	GEXP_TXP_1	C389	0.1UF	GEXP_TXP_C_1
8	GEXP_TXN_1	C390	0.1UF	GEXP_TXN_C_1
8	GEXP_TXP_2	C377	0.1UF	GEXP_TXP_C_2
8	GEXP_TXN_2	C378	0.1UF	GEXP_TXN_C_2
8	GEXP_TXP_3	C379	0.1UF	GEXP_TXP_C_3
8	GEXP_TXN_3	C380	0.1UF	GEXP_TXN_C_3
8	GEXP_TXP_4	C381	0.1UF	GEXP_TXP_C_4
8	GEXP_TXN_4	C382	0.1UF	GEXP_TXN_C_4
8	GEXP_TXP_5	C383	0.1UF	GEXP_TXP_C_5
8	GEXP_TXN_5	C384	0.1UF	GEXP_TXN_C_5
8	GEXP_TXP_6	C385	0.1UF	GEXP_TXP_C_6
8	GEXP_TXN_6	C386	0.1UF	GEXP_TXN_C_6
8	GEXP_TXP_7	C387	0.1UF	GEXP_TXP_C_7
8	GEXP_TXN_7	C388	0.1UF	GEXP_TXN_C_7

V0.2

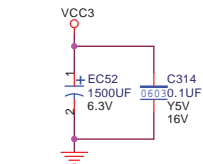
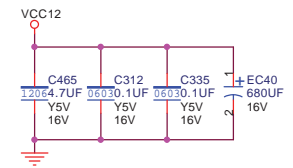
16	GEXP_0_TXP_SW_8	B50	HSOP8(I)	RSVD_7(B)	A50	
16	GEXP_0_TXN_SW_8	B51	HSOP8(I)	GND_53(P)	A51	
16	GEXP_0_TXP_SW_9	B52	GND_38(P)	HSIP8(O)	A52	<<GEXP_0_RXP_SW_8 16
16	GEXP_0_TXN_SW_9	B53	GND_39(P)	HSIN8(O)	A53	<<GEXP_0_RXN_SW_8 16
16	GEXP_0_TXP_SW_10	B54	HSOP9(I)	GND_54(P)	A54	
16	GEXP_0_TXN_SW_10	B55	HSOP9(I)	GND_55(P)	A55	
16	GEXP_0_TXP_SW_11	B56	GND_40(P)	HSIP9(O)	A56	<<GEXP_0_RXP_SW_9 16
16	GEXP_0_TXN_SW_11	B57	GND_41(P)	HSIN9(O)	A57	<<GEXP_0_RXN_SW_9 16
16	GEXP_0_TXP_SW_12	B58	HSOP10(I)	GND_56(P)	A58	
16	GEXP_0_TXN_SW_12	B59	HSOP10(I)	GND_57(P)	A59	
16	GEXP_0_TXP_SW_13	B60	GND_42(P)	HSIP10(O)	A60	<<GEXP_0_RXP_SW_10 16
16	GEXP_0_TXN_SW_13	B61	GND_43(P)	HSIN10(O)	A61	<<GEXP_0_RXN_SW_10 16
16	GEXP_0_TXP_SW_14	B62	HSOP11(I)	GND_58(P)	A62	
16	GEXP_0_TXN_SW_14	B63	HSOP11(I)	GND_59(P)	A63	
16	GEXP_0_TXP_SW_15	B64	GND_44(P)	HSIP11(O)	A64	<<GEXP_0_RXP_SW_11 16
16	GEXP_0_TXN_SW_15	B65	GND_45(P)	HSIN11(O)	A65	<<GEXP_0_RXN_SW_11 16
16	GEXP_0_TXP_SW_16	B66	HSOP12(I)	GND_60(P)	A66	
16	GEXP_0_TXN_SW_16	B67	HSOP12(I)	GND_61(P)	A67	
16	GEXP_0_TXP_SW_17	B68	GND_46(P)	HSIP12(O)	A68	<<GEXP_0_RXP_SW_12 16
16	GEXP_0_TXN_SW_17	B69	GND_47(P)	HSIN12(O)	A69	<<GEXP_0_RXN_SW_12 16
16	GEXP_0_TXP_SW_18	B70	HSOP13(I)	GND_62(P)	A70	
16	GEXP_0_TXN_SW_18	B71	HSOP13(I)	GND_63(P)	A71	
16	GEXP_0_TXP_SW_19	B72	GND_48(P)	HSIP13(O)	A72	<<GEXP_0_RXP_SW_13 16
16	GEXP_0_TXN_SW_19	B73	GND_49(P)	HSIN13(O)	A73	<<GEXP_0_RXN_SW_13 16
16	GEXP_0_TXP_SW_20	B74	HSOP14(I)	GND_64(P)	A74	
16	GEXP_0_TXN_SW_20	B75	HSOP14(I)	GND_65(P)	A75	
16	GEXP_0_TXP_SW_21	B76	GND_50(P)	HSIP14(O)	A76	<<GEXP_0_RXP_SW_14 16
16	GEXP_0_TXN_SW_21	B77	GND_51(P)	HSIN14(O)	A77	<<GEXP_0_RXN_SW_14 16
16	GEXP_0_TXP_SW_22	B78	HSOP15(I)	GND_66(P)	A78	
16	GEXP_0_TXN_SW_22	B79	HSOP15(I)	GND_67(P)	A79	
16	GEXP_0_TXP_SW_23	B80	GND_52(P)	HSIP15(O)	A80	<<GEXP_0_RXP_SW_15 16
16	GEXP_0_TXN_SW_23	B81	GND_53(P)	HSIN15(O)	A81	<<GEXP_0_RXN_SW_15 16
8	PRIPRSNT#	B82	PRSNT2#_4(I)	RSVD_6(I)	A82	

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PCIE164
SL-PCIE164P

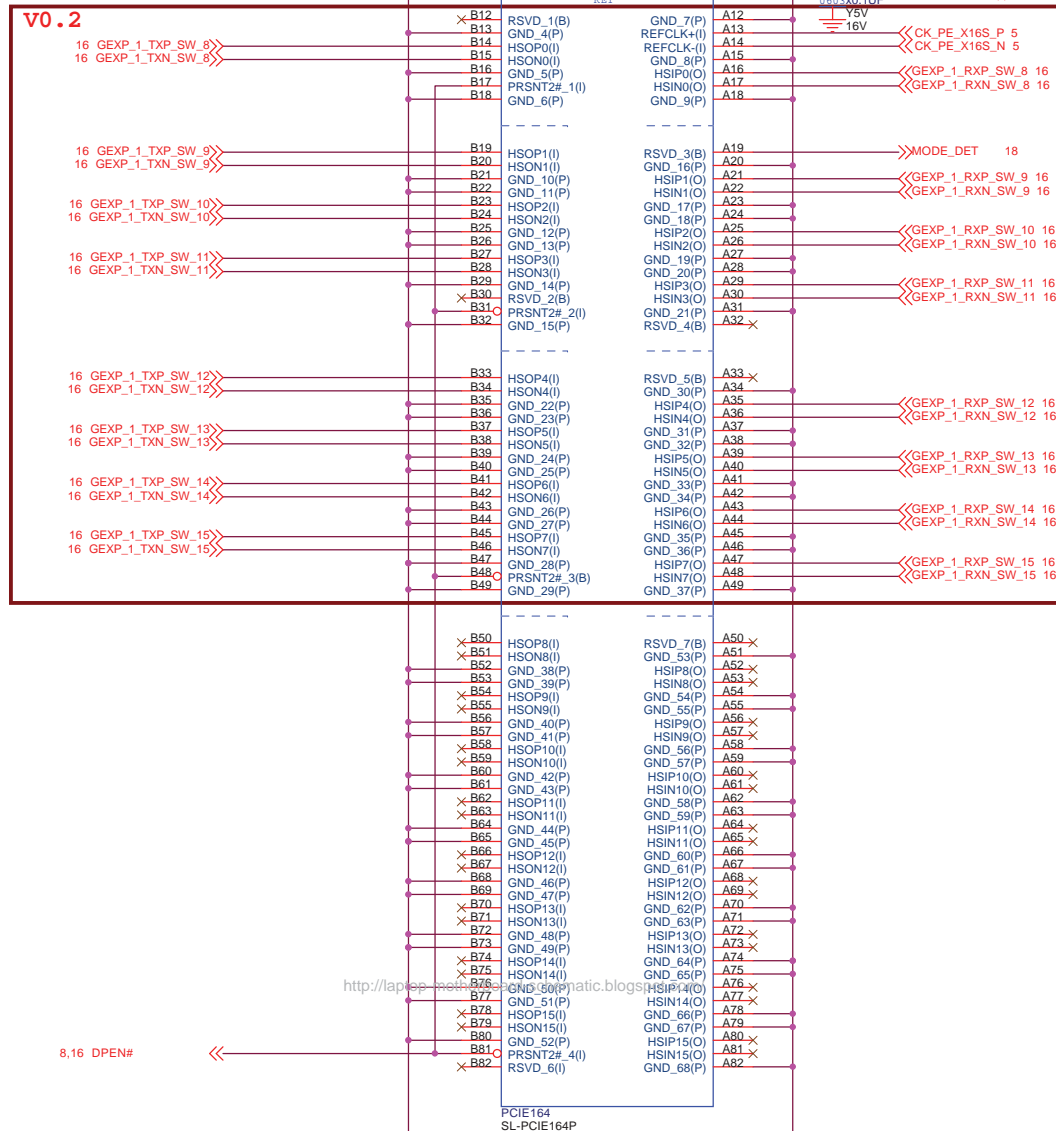
PCIE_RST#	<<PCIE_RST#	15,20,27
WAKE#	>>WAKE#	15,18,20

SMBDATA	<<SMBDATA	11,12,15,18,20,25,26
SMBCLK	<<SMBCLK	11,12,15,18,20,25,26



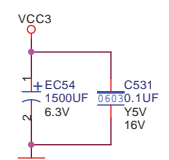
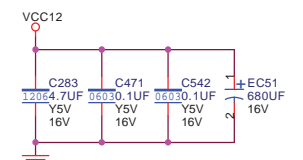
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Title : PCI EXPRESS X16 SLOT MASTER	Page : 14 / 35
Document Number : M514	Rev : 0.2
Date : Monday, December 19, 2005	Size : 16.8" X 11.8"



PCIE_RST# << PCIE_RST# 14,20,27
WAKE# >> WAKE# 14,18,20

SMBDATA <<>> SMBDATA 11,12,14,18,20,25,26
SMBCLK <<>> SMBCLK 11,12,14,18,20,25,26



V0.2 Add this Page Circuit

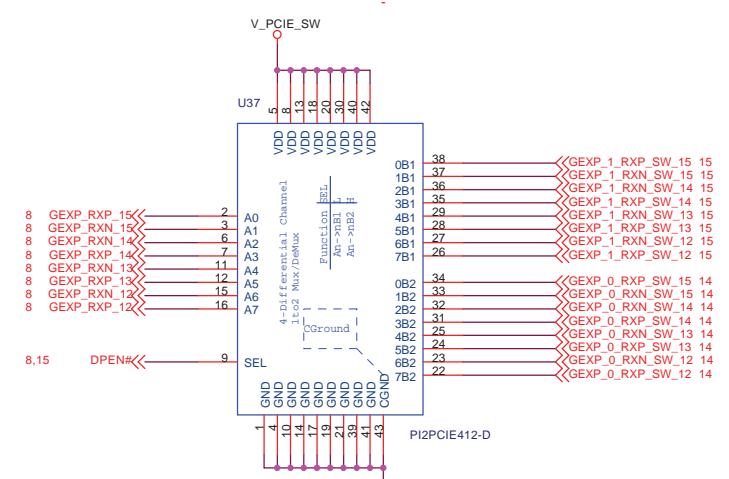
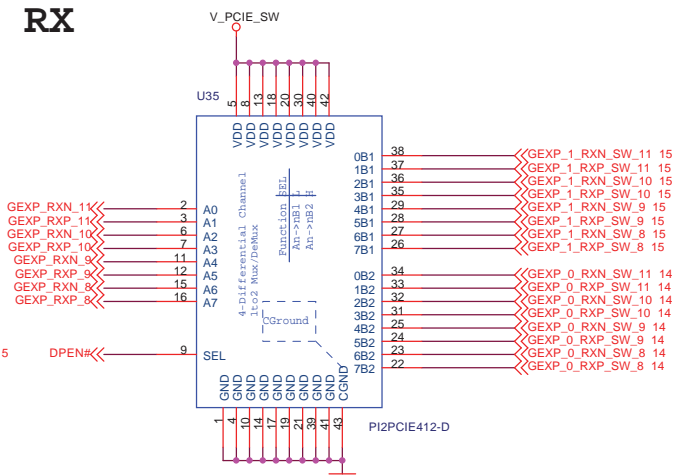
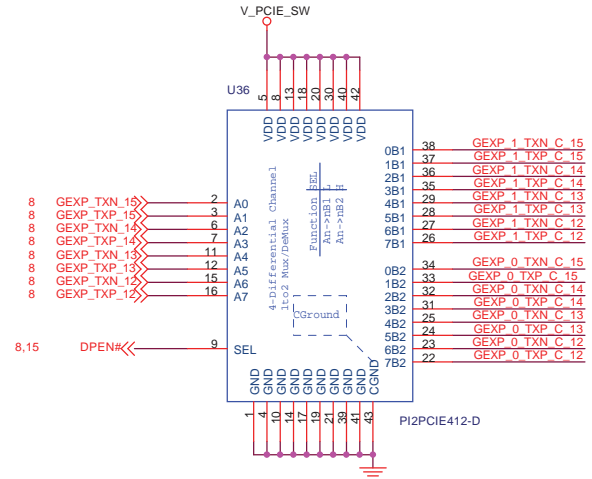
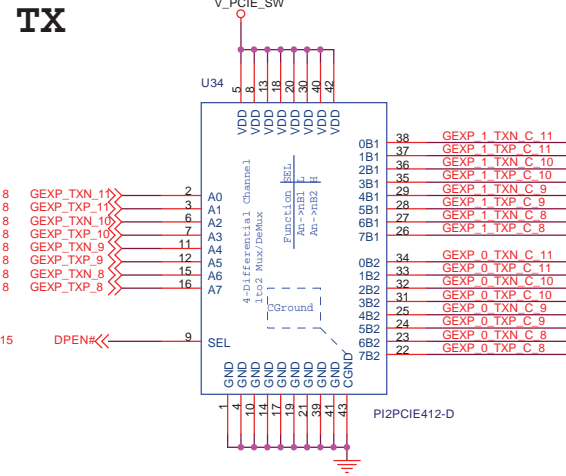
14 GEXP_0_TXP_SW_8>>	C256	0.1UF	GEXP_0_TXP_C_8
14 GEXP_0_TXN_SW_8>>	C258	0.1UF	GEXP_0_TXN_C_8
14 GEXP_0_TXP_SW_9>>	C260	0.1UF	GEXP_0_TXP_C_9
14 GEXP_0_TXN_SW_9>>	C262	0.1UF	GEXP_0_TXN_C_9
14 GEXP_0_TXP_SW_10>>	C259	0.1UF	GEXP_0_TXP_C_10
14 GEXP_0_TXN_SW_10>>	C261	0.1UF	GEXP_0_TXN_C_10
14 GEXP_0_TXP_SW_11>>	C263	0.1UF	GEXP_0_TXP_C_11
14 GEXP_0_TXN_SW_11>>	C266	0.1UF	GEXP_0_TXN_C_11

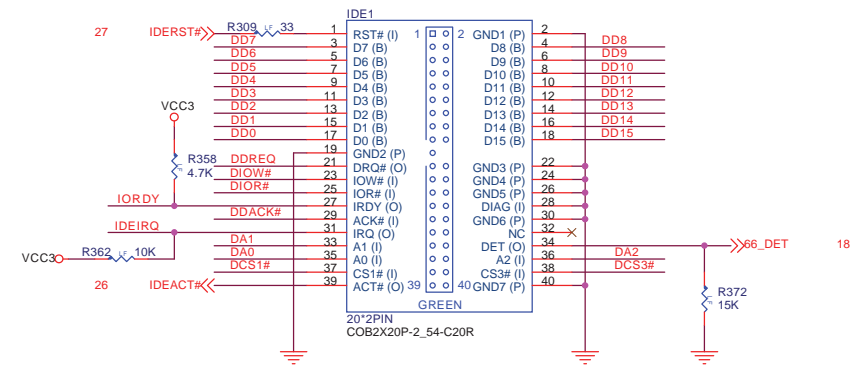
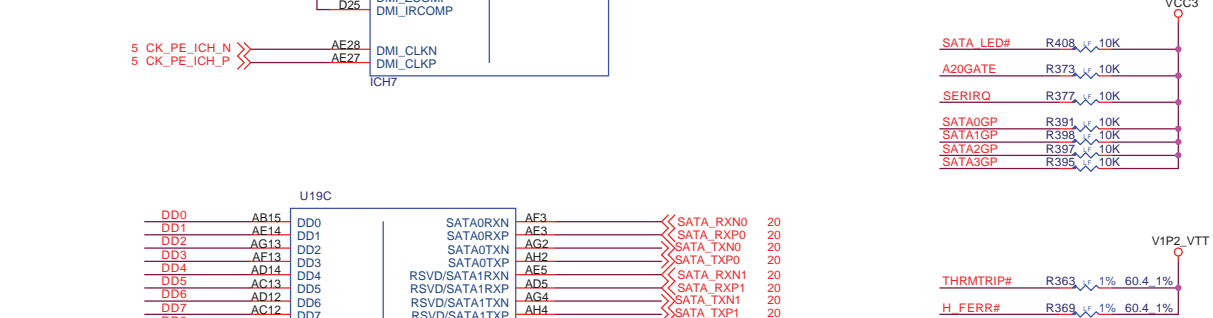
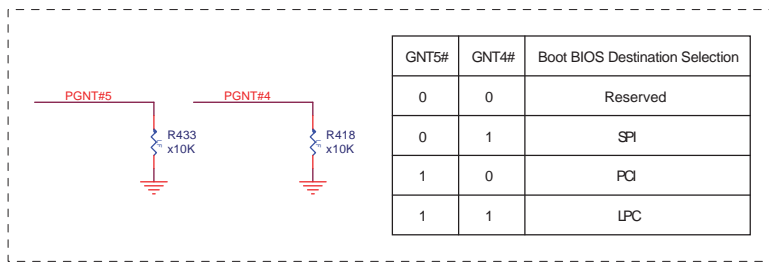
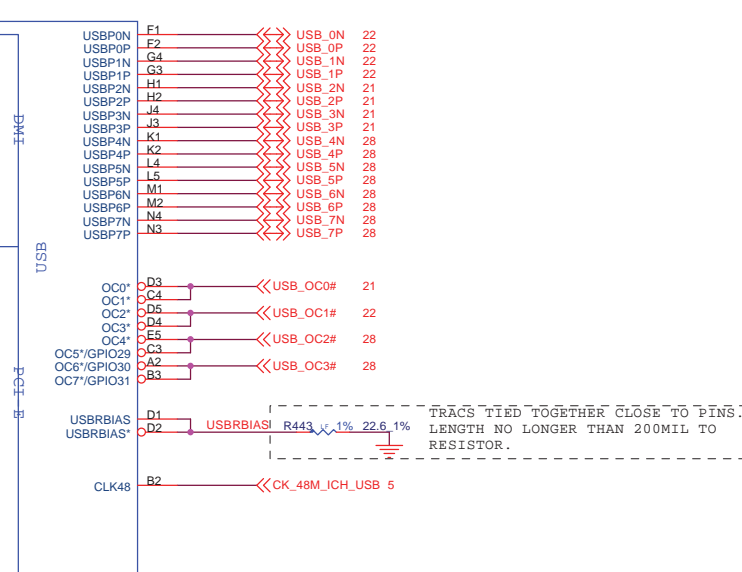
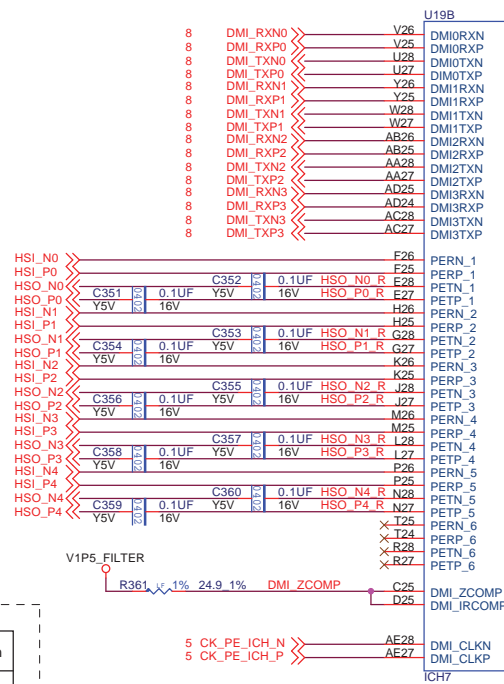
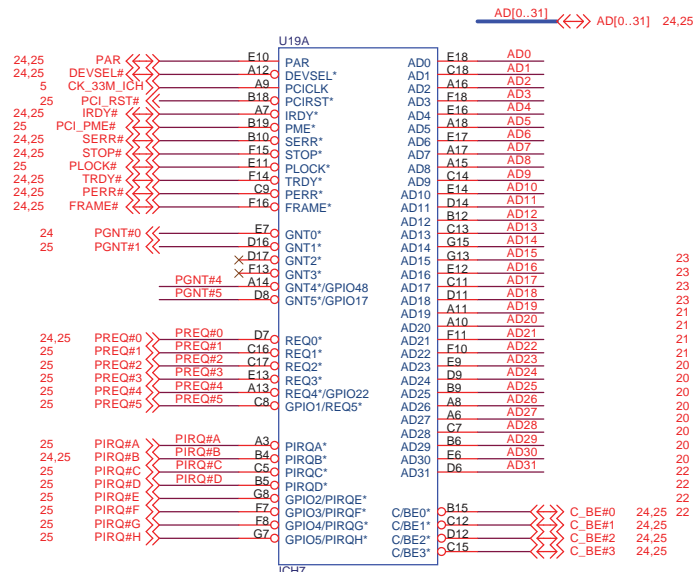
14 GEXP_0_TXP_SW_12>>	C267	0.1UF	GEXP_0_TXP_C_12
14 GEXP_0_TXN_SW_12>>	C272	0.1UF	GEXP_0_TXN_C_12
14 GEXP_0_TXP_SW_13>>	C264	0.1UF	GEXP_0_TXP_C_13
14 GEXP_0_TXN_SW_13>>	C265	0.1UF	GEXP_0_TXN_C_13
14 GEXP_0_TXP_SW_14>>	C274	0.1UF	GEXP_0_TXP_C_14
14 GEXP_0_TXN_SW_14>>	C273	0.1UF	GEXP_0_TXN_C_14
14 GEXP_0_TXP_SW_15>>	C276	0.1UF	GEXP_0_TXP_C_15
14 GEXP_0_TXN_SW_15>>	C277	0.1UF	GEXP_0_TXN_C_15

15 GEXP_1_TXP_SW_8>>	C598	0.1UF	GEXP_1_TXP_C_8
15 GEXP_1_TXN_SW_8>>	C599	0.1UF	GEXP_1_TXN_C_8
15 GEXP_1_TXP_SW_9>>	C600	0.1UF	GEXP_1_TXP_C_9
15 GEXP_1_TXN_SW_9>>	C601	0.1UF	GEXP_1_TXN_C_9
15 GEXP_1_TXP_SW_10>>	C602	0.1UF	GEXP_1_TXP_C_10
15 GEXP_1_TXN_SW_10>>	C603	0.1UF	GEXP_1_TXN_C_10
15 GEXP_1_TXP_SW_11>>	C604	0.1UF	GEXP_1_TXP_C_11
15 GEXP_1_TXN_SW_11>>	C605	0.1UF	GEXP_1_TXN_C_11

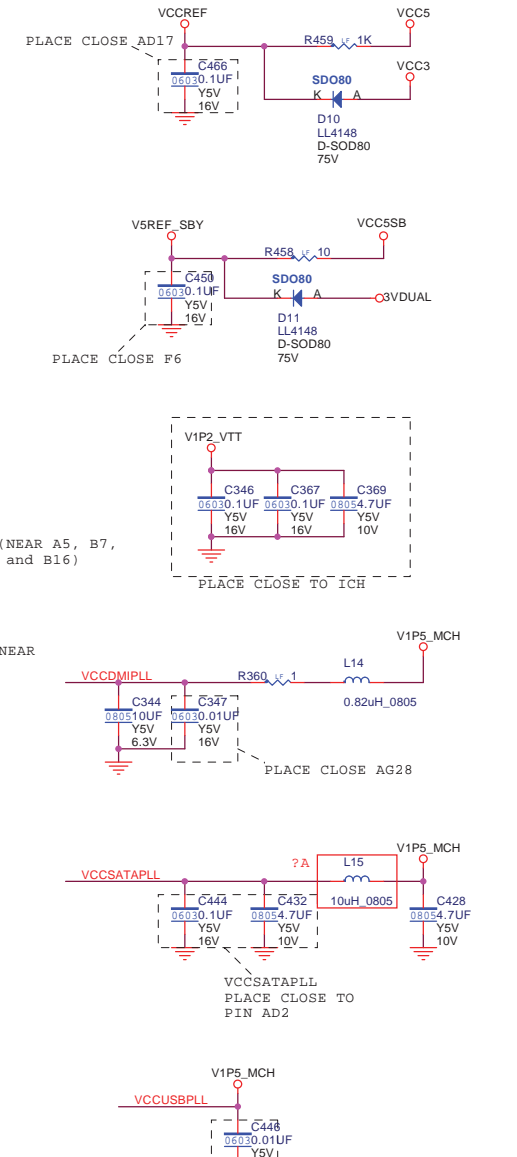
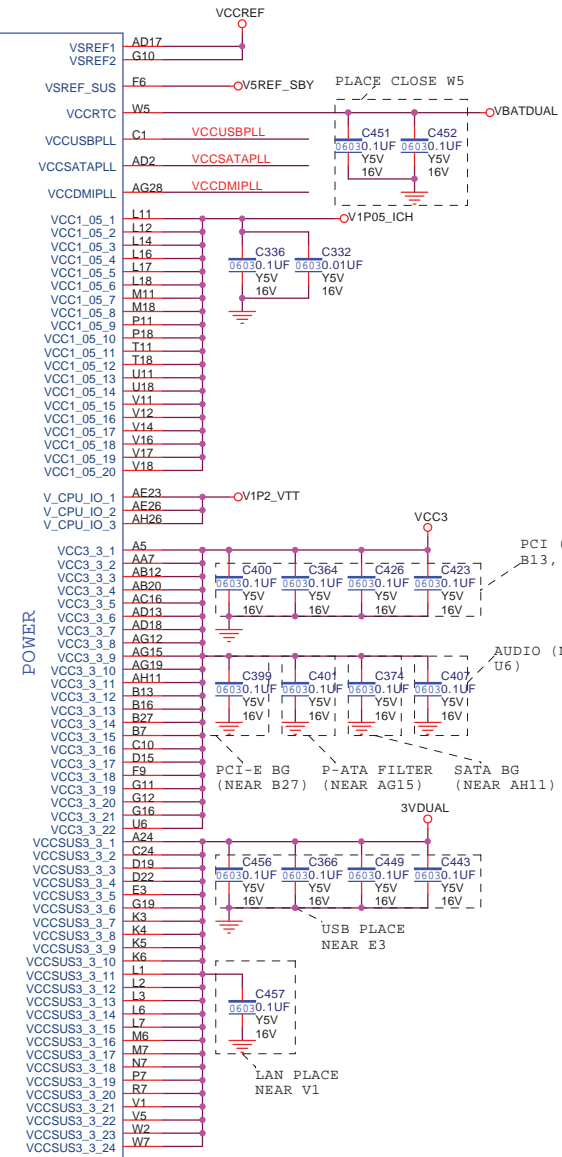
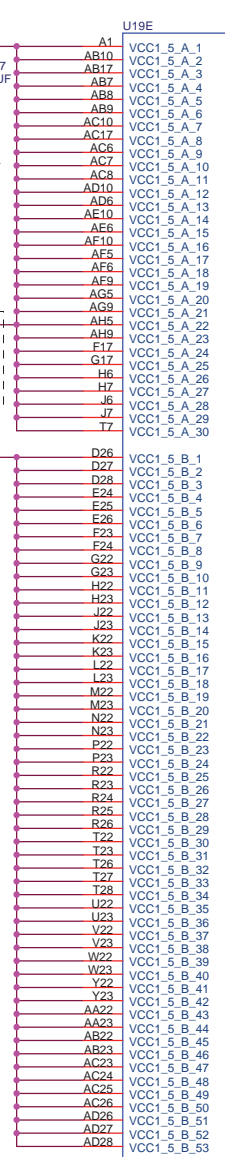
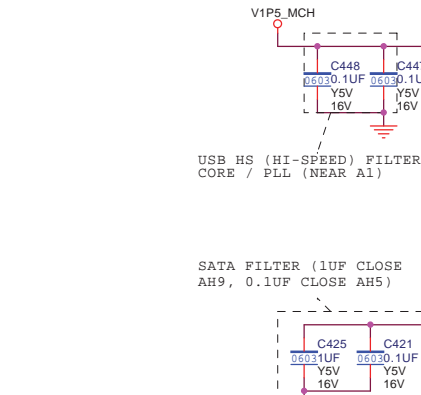
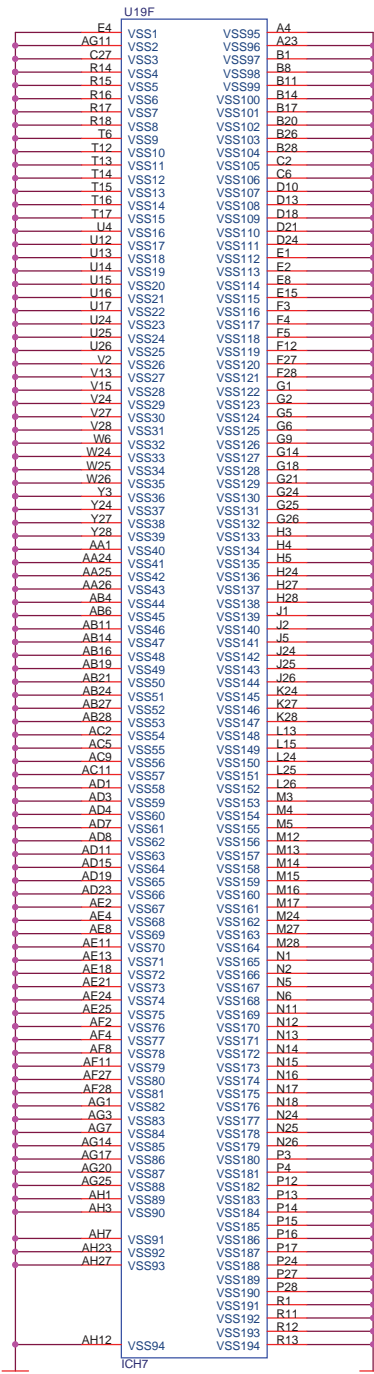
15 GEXP_1_TXP_SW_12>>	C606	0.1UF	GEXP_1_TXP_C_12
15 GEXP_1_TXN_SW_12>>	C607	0.1UF	GEXP_1_TXN_C_12
15 GEXP_1_TXP_SW_13>>	C608	0.1UF	GEXP_1_TXP_C_13
15 GEXP_1_TXN_SW_13>>	C609	0.1UF	GEXP_1_TXN_C_13
15 GEXP_1_TXP_SW_14>>	C610	0.1UF	GEXP_1_TXP_C_14
15 GEXP_1_TXN_SW_14>>	C611	0.1UF	GEXP_1_TXN_C_14
15 GEXP_1_TXP_SW_15>>	C612	0.1UF	GEXP_1_TXP_C_15
15 GEXP_1_TXN_SW_15>>	C613	0.1UF	GEXP_1_TXN_C_15

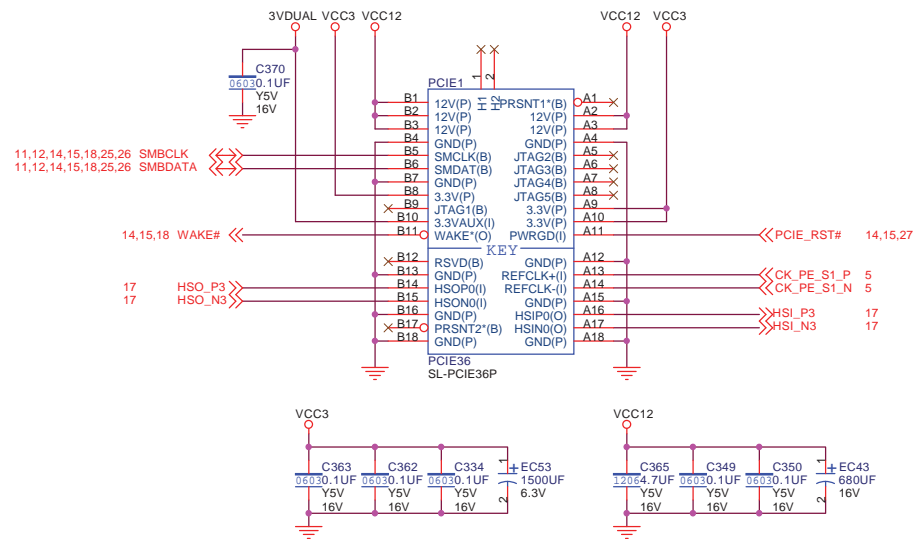
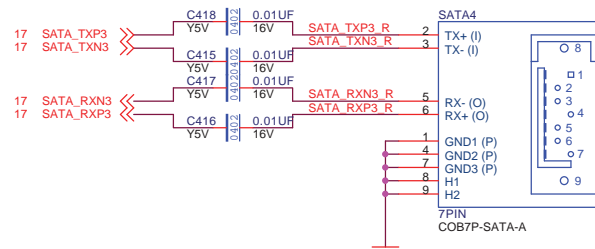
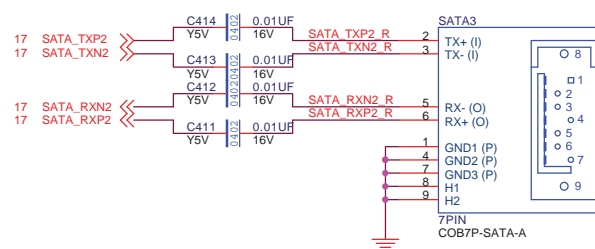
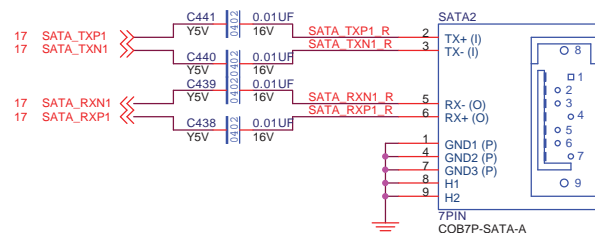
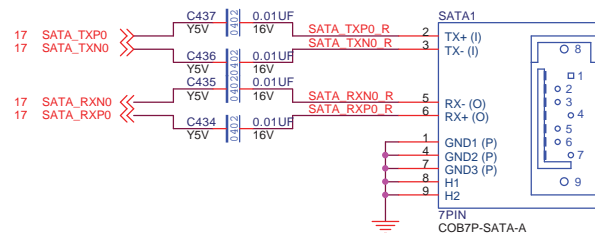
Place Caps near Connector
within 600 mils



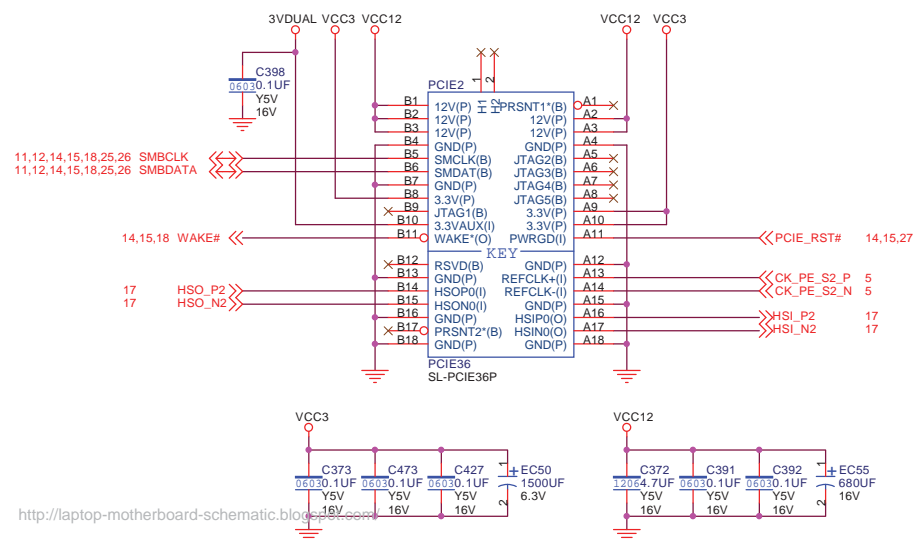


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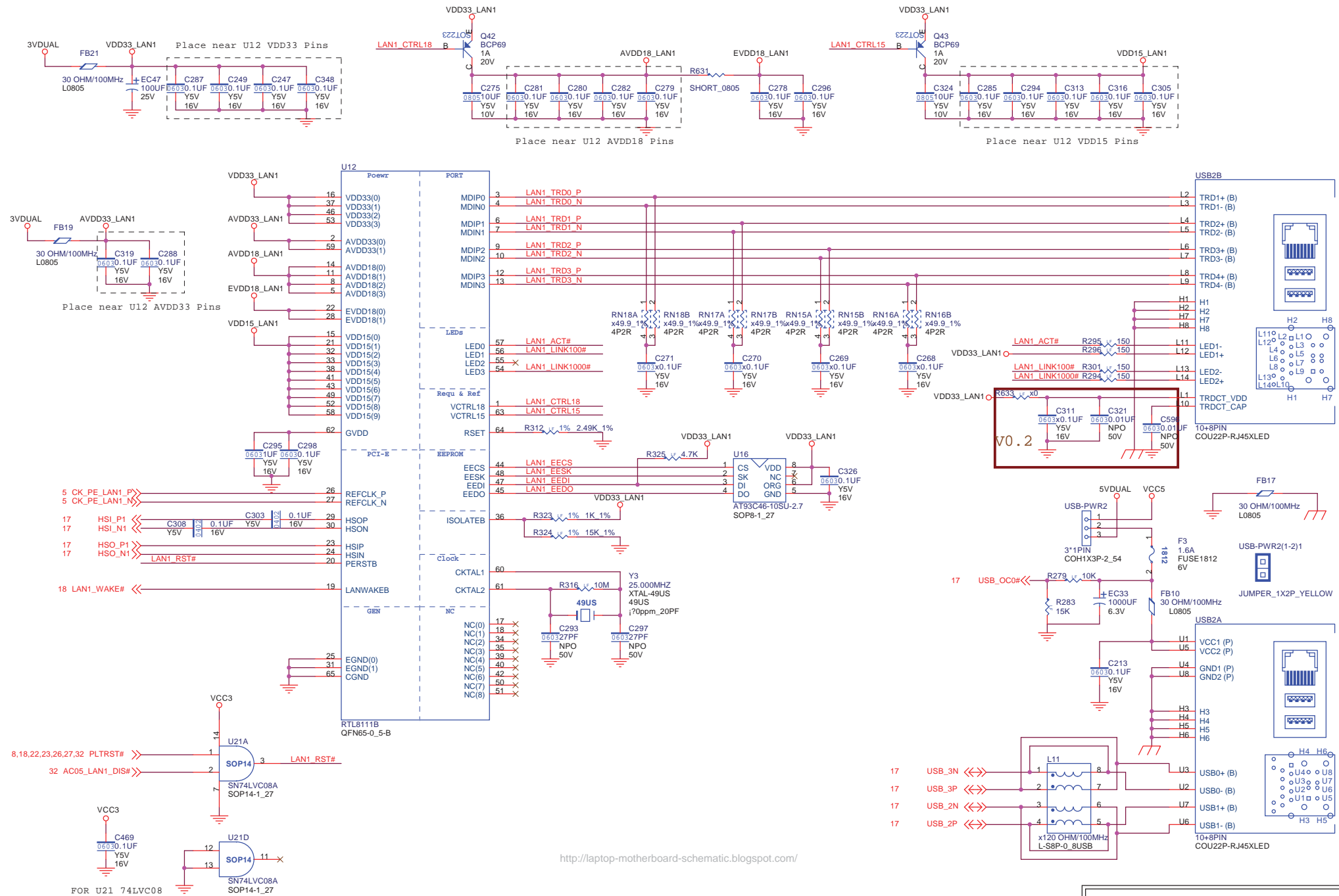




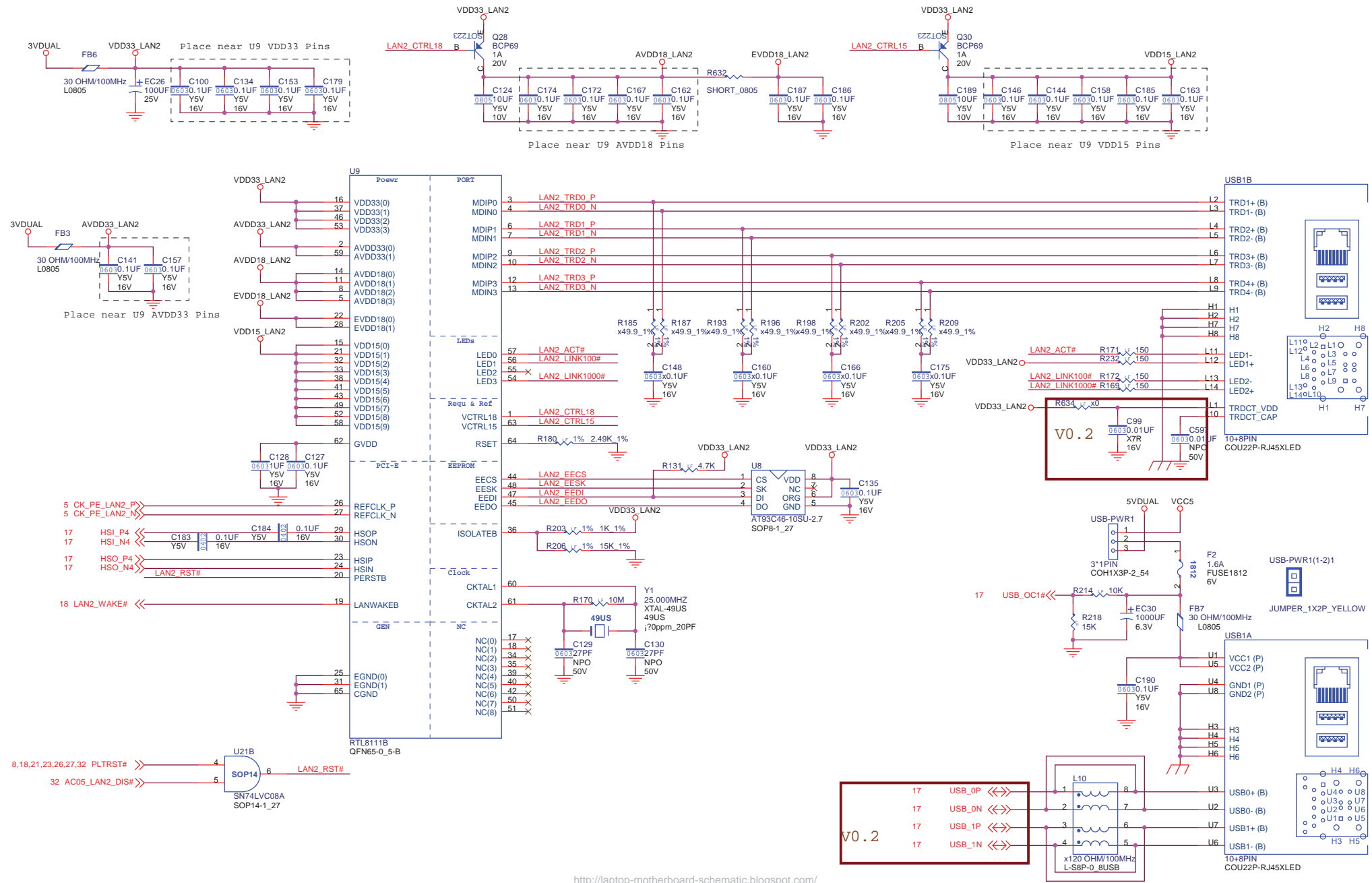
FOR PCI EXPRESS X1 SLOT 1



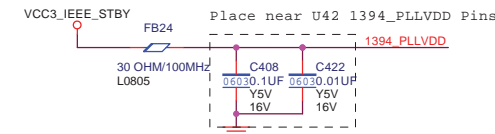
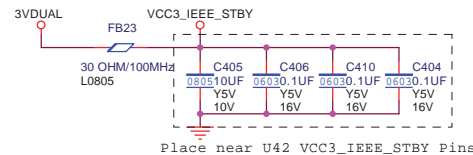
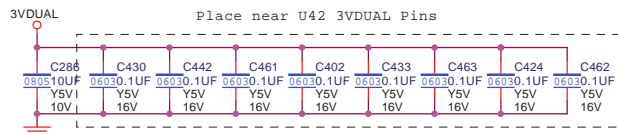
FOR PCI EXPRESS X1 SLOT 2



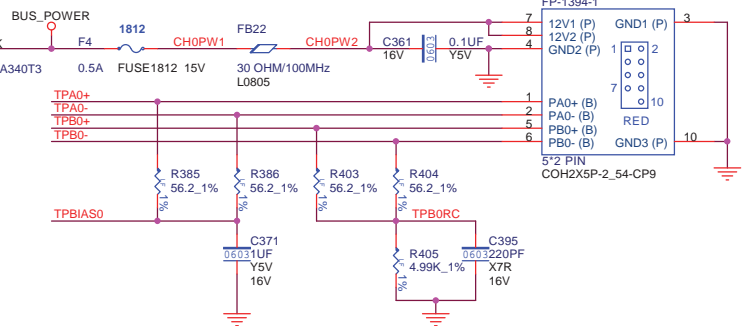
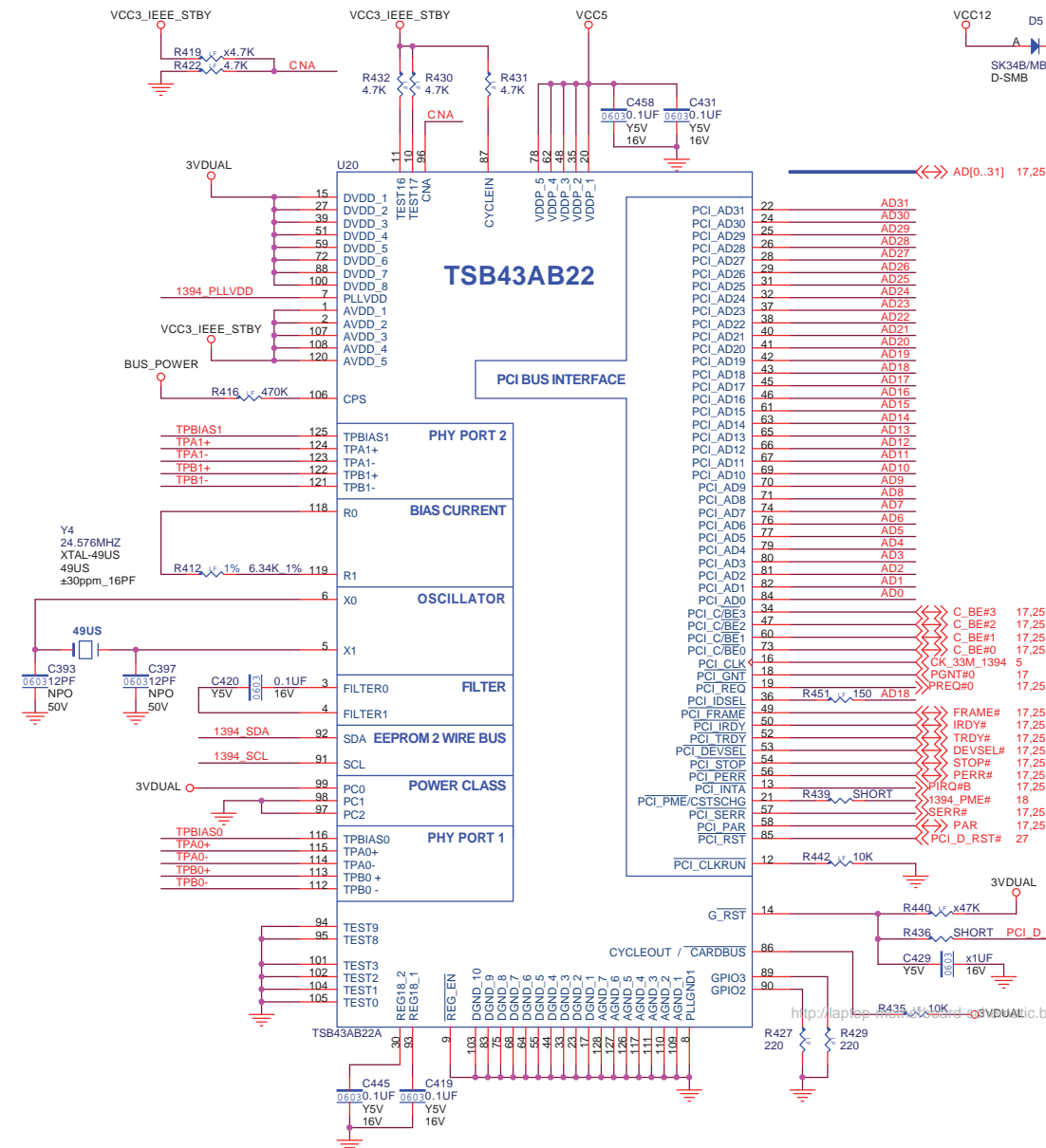
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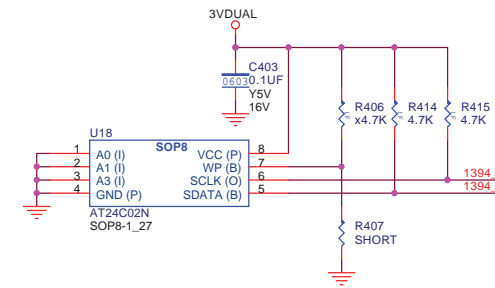
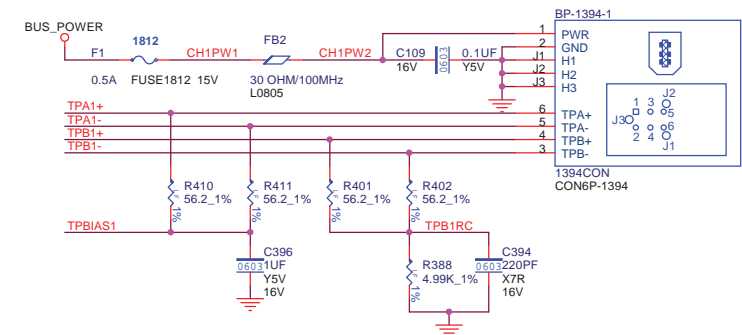
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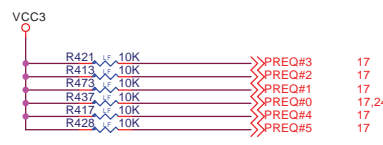
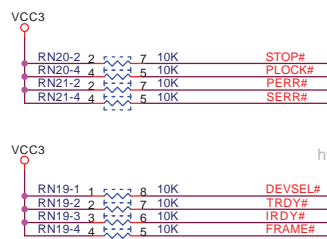
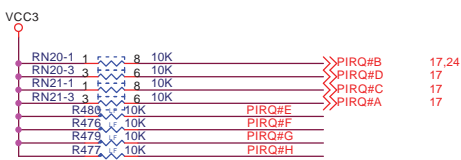
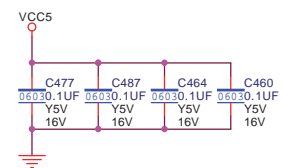
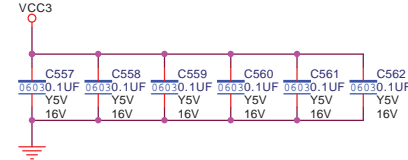
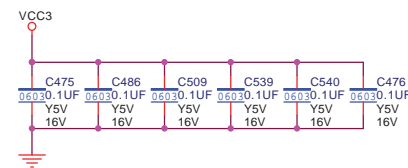
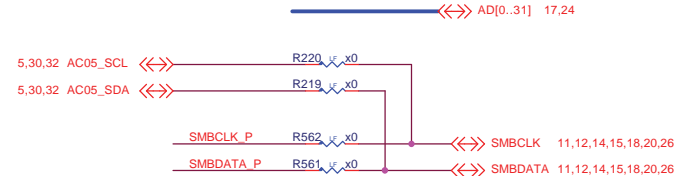
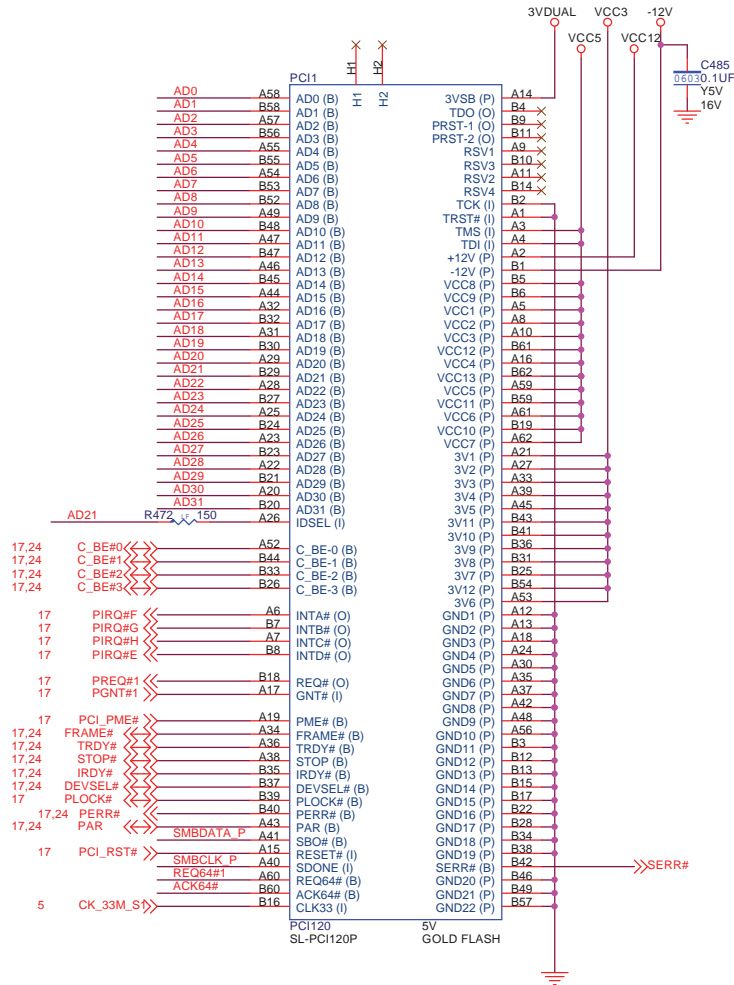


IEEE-1394 Channel 0

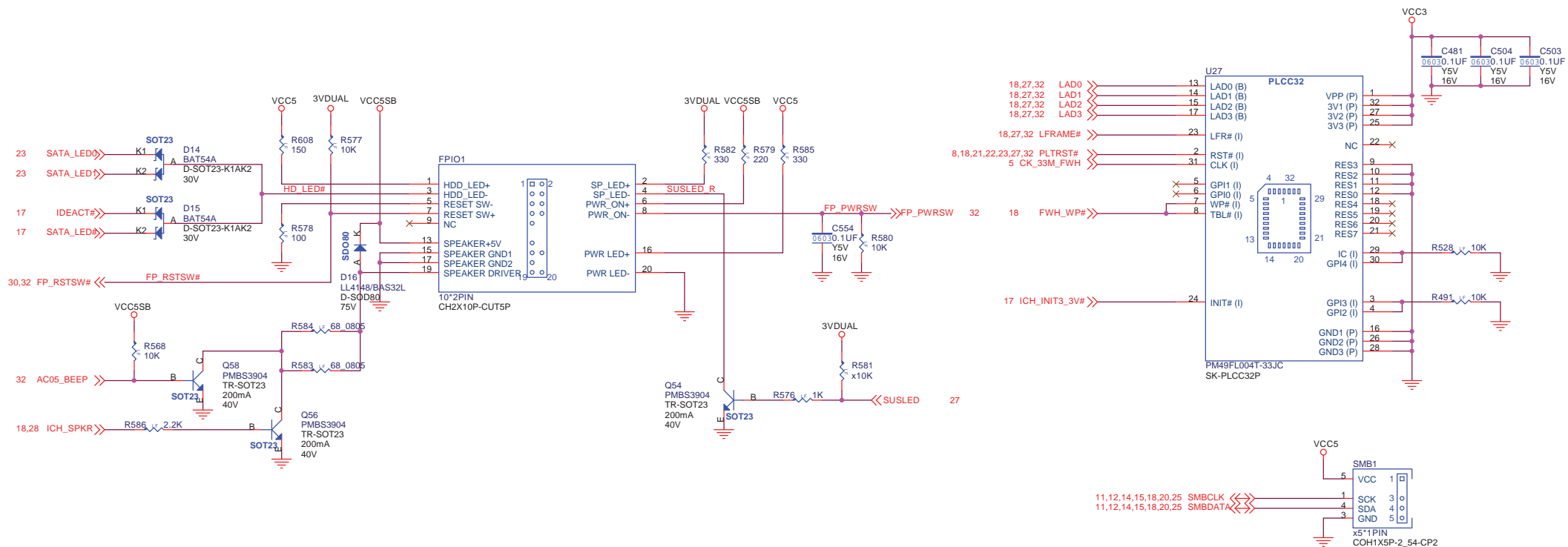
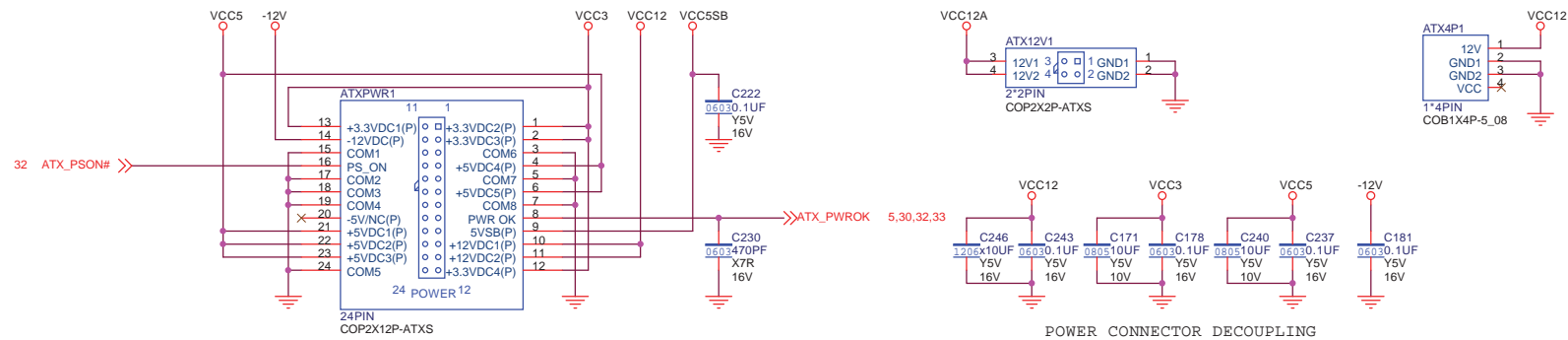


IEEE-1394 Channel 1

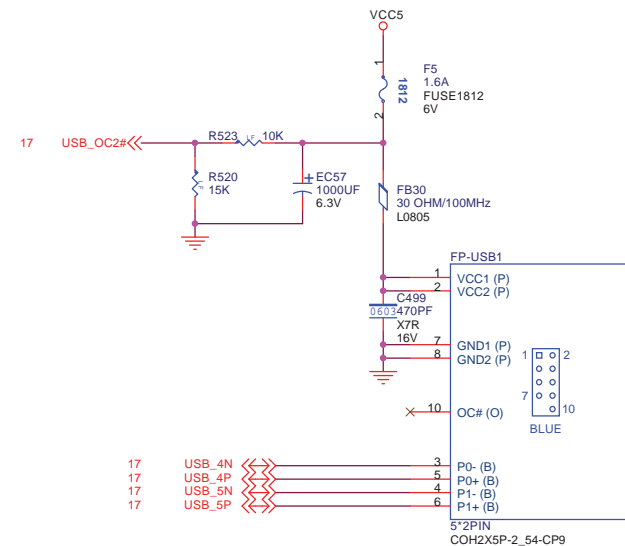
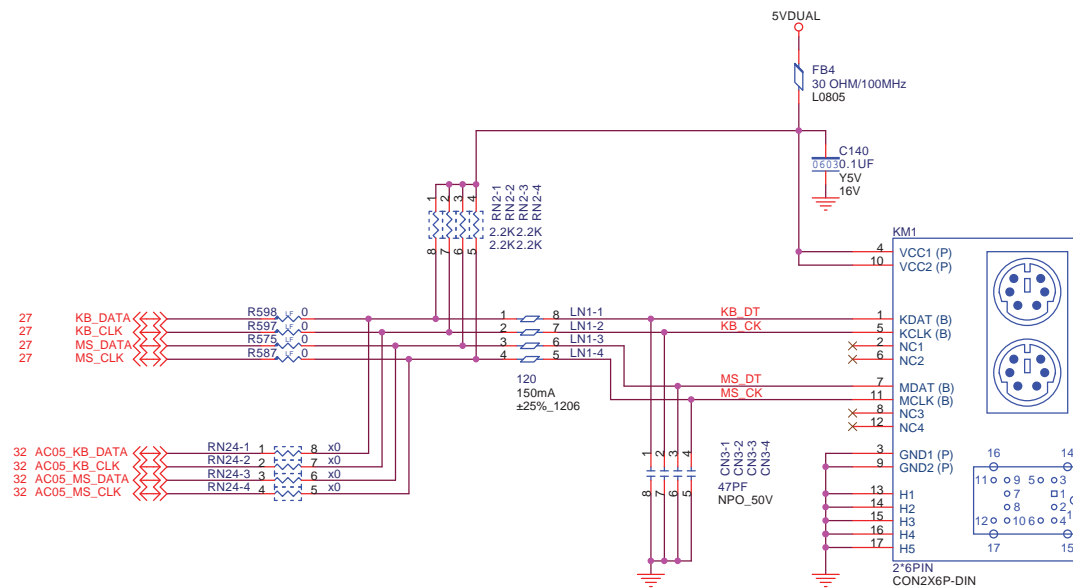




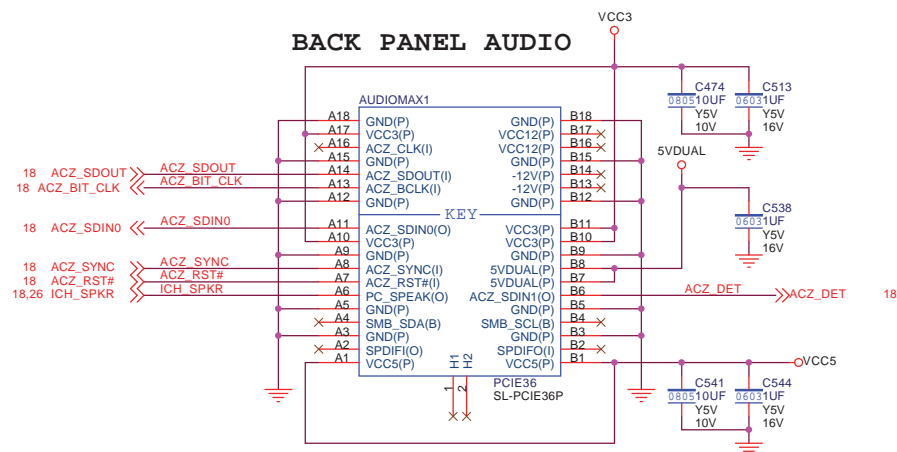
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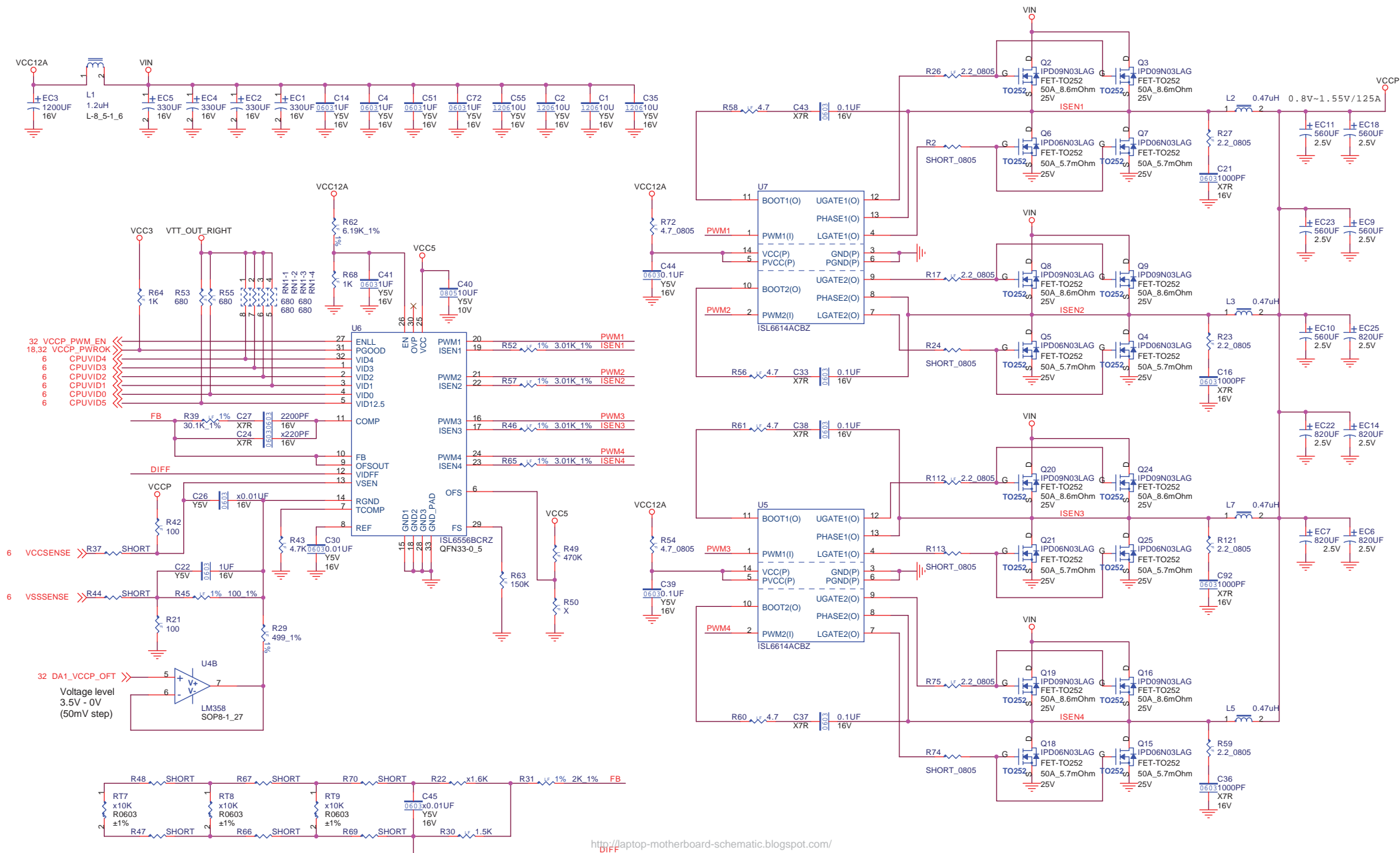


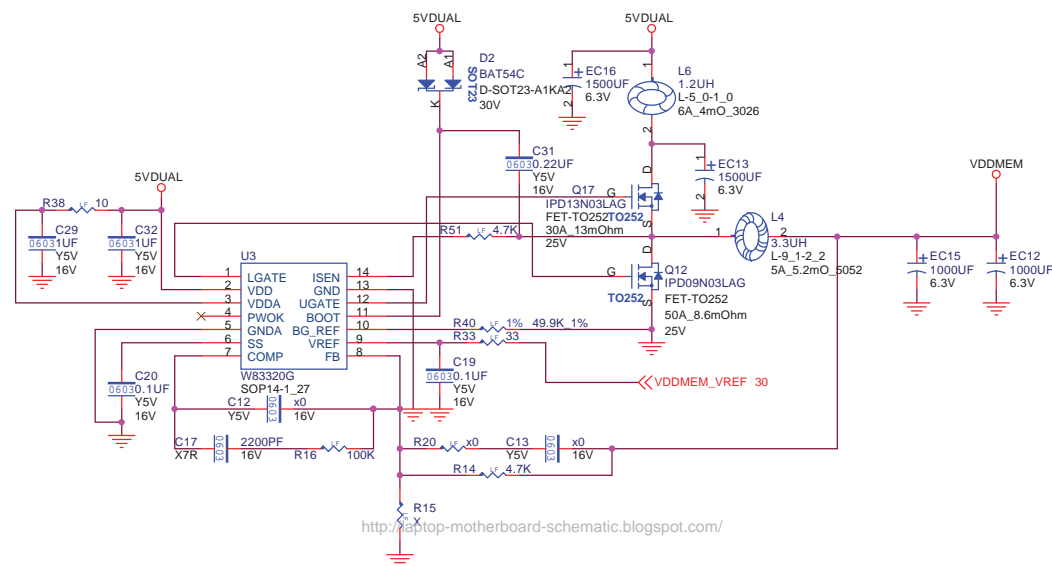
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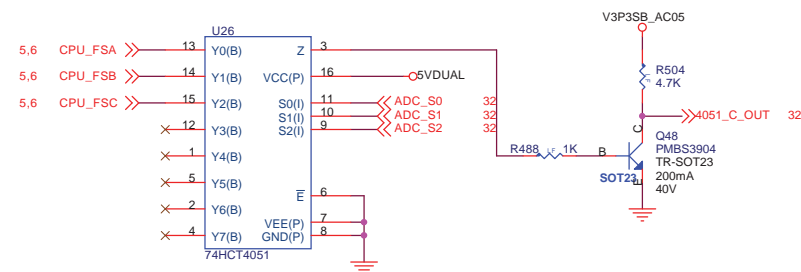
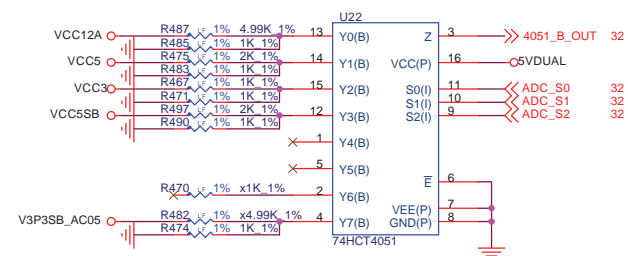
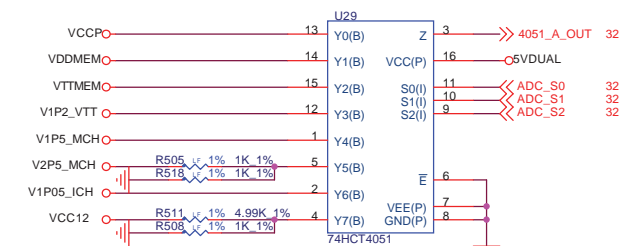
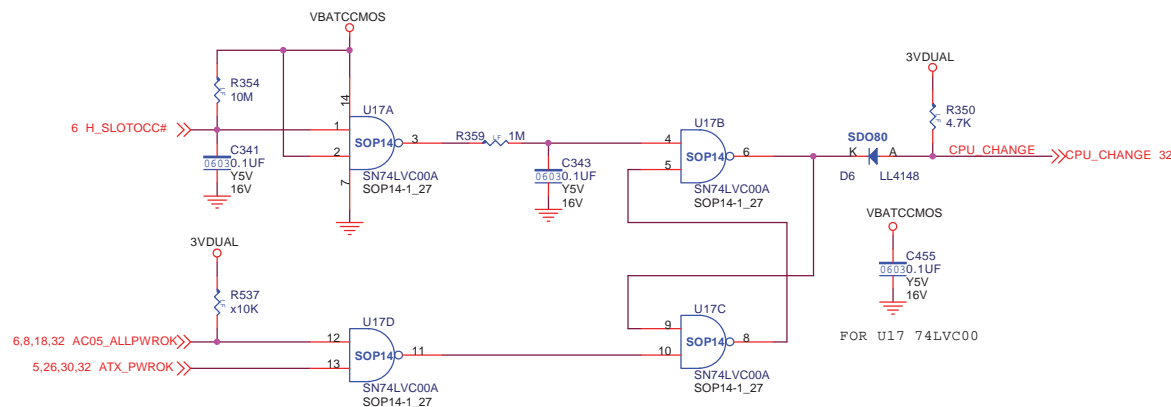
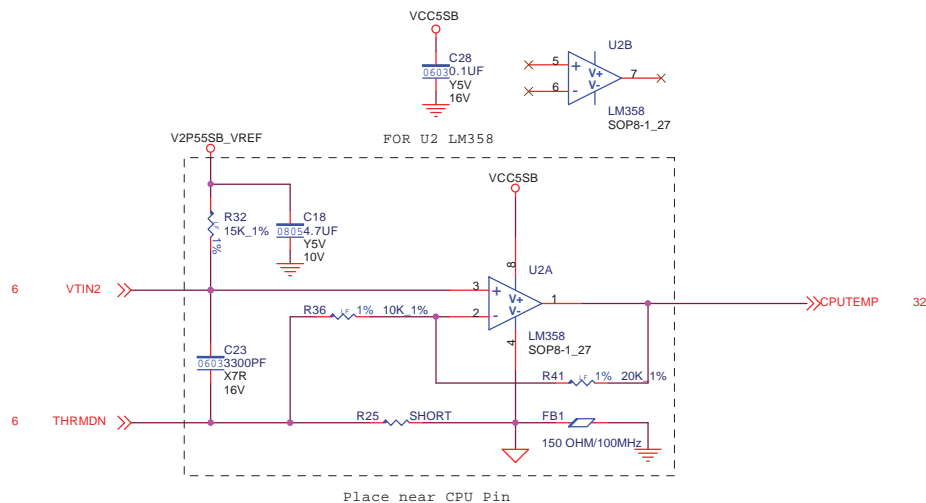


BACK PANEL AUDIO

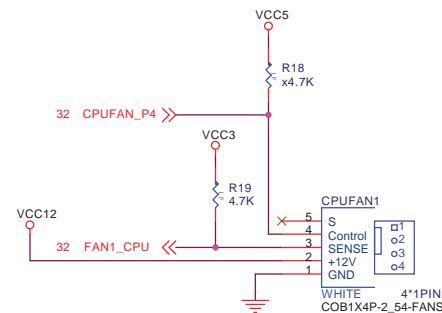
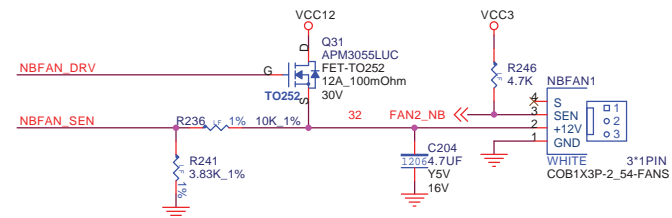
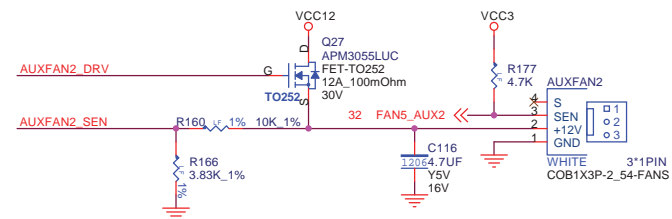
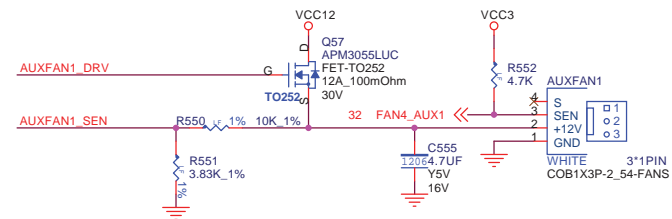
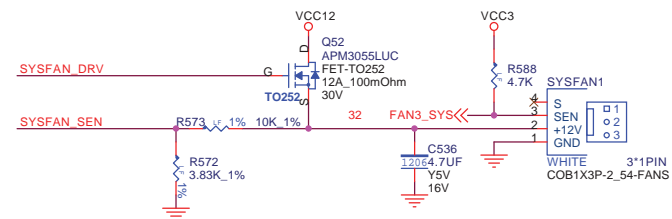
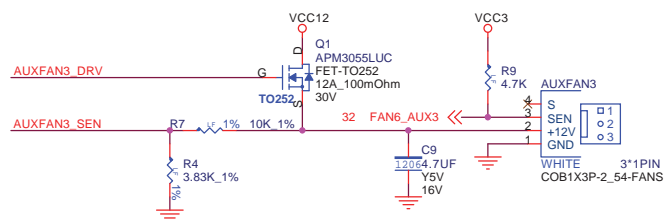
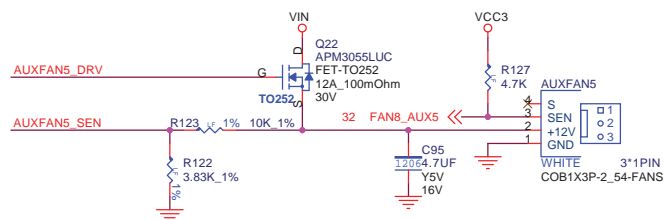
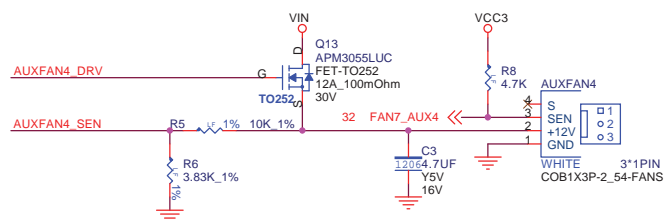
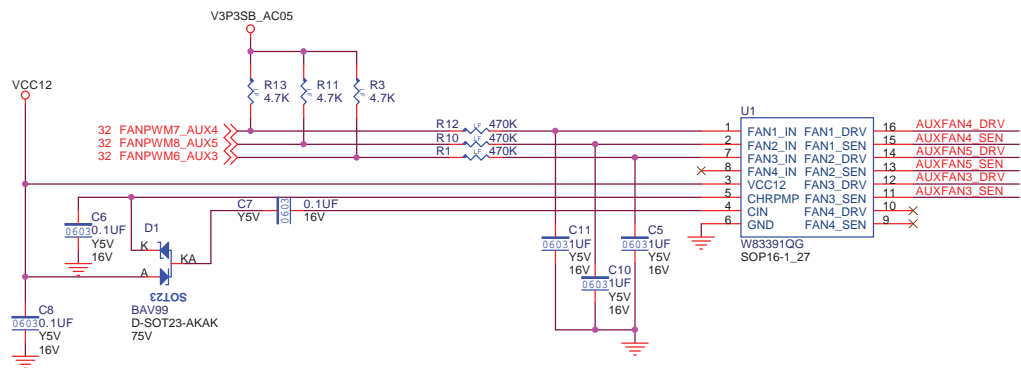
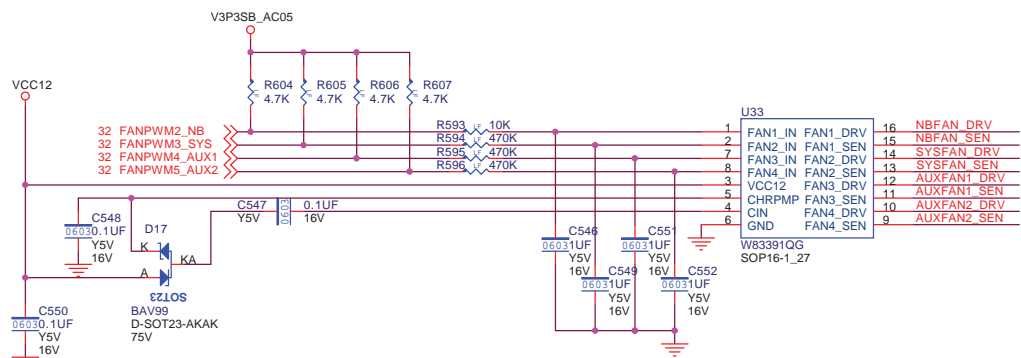




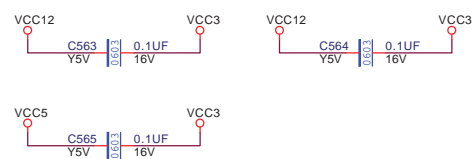
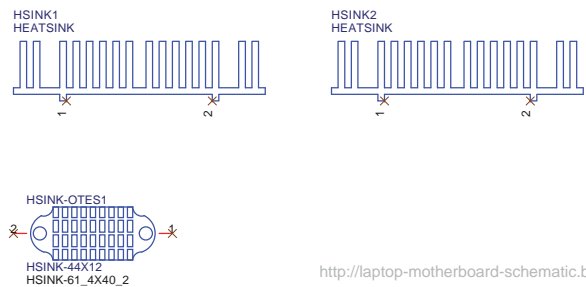
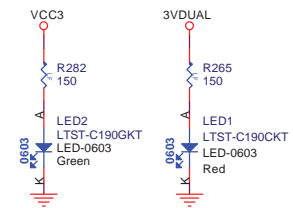
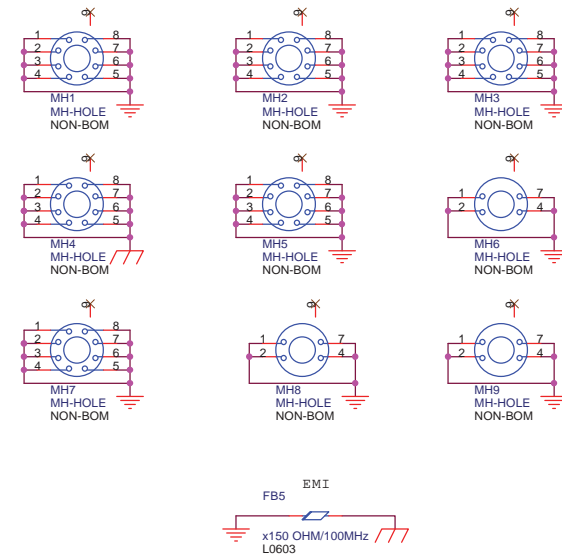
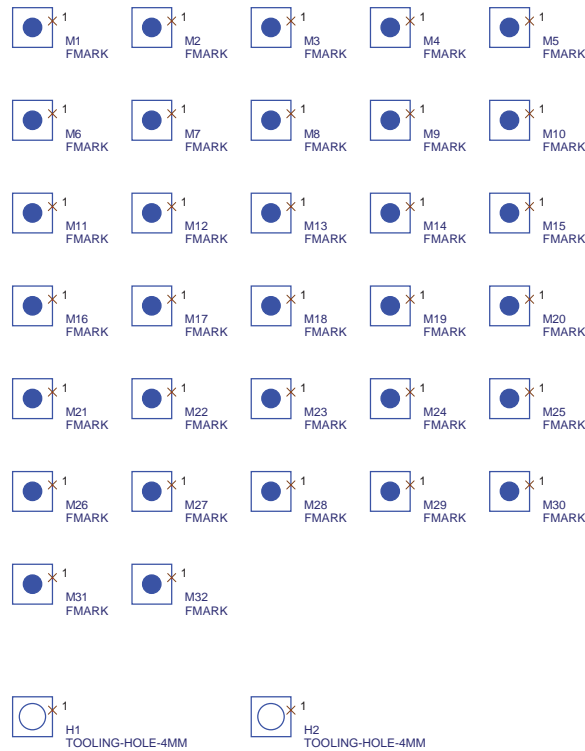
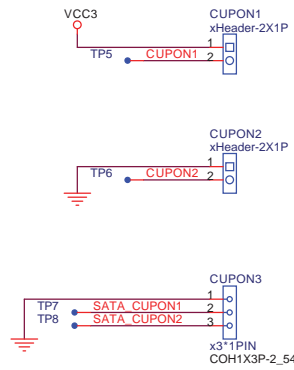




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